EECS 370 Discussion

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EECS 370 Discussion

Topics Today:

- 5-stage Pipeline
  - Basic Design
  - Performance
  - Data Hazards
- Exams

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Single Cycle

CPI =

Clock Period =

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Single Cycle	Multi-Cycle
CPI = 1	CPI =
Clock Period = long	Clock Period =

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Single Cycle	Multi-Cycle	Pipelined
CPI = 1	CPI = >1	CPI =
Clock Period = long	Clock Period = short	Clock Period =

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Single Cycle	Multi-Cycle	Pipelined
CPI = 1	CPI = >1	CPI ≈ 1
Clock Period = long	Clock Period = short	Clock Period = short

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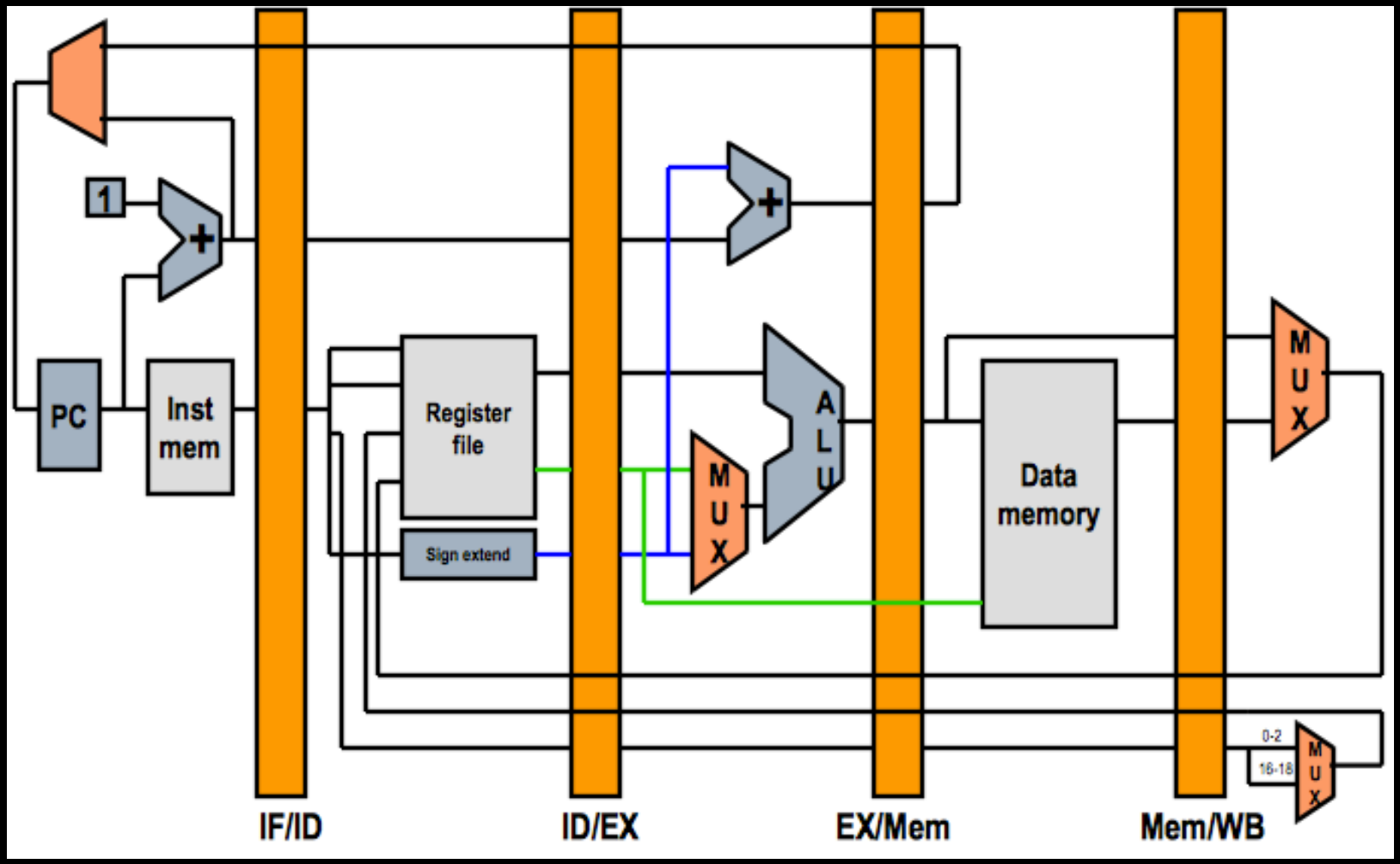
5-stage Pipeline



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5-stage Pipeline

Pipeline Example

```
add  1  2  3
nand 4  5  6
lw   0  4  26
add  2  2  2
nand 1  1  1
```

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5-stage Pipeline

Key Concept

1000 instructions are run on a 5-stage pipeline (no hazards)

How many cycles are needed to complete them?

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5-stage Pipeline

Key Concept

1000 instructions are run on a 5-stage pipeline (no hazards)
How many cycles are needed to complete them?

1004 cycles

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Multi-Cycle Datapath

Timing Example

100 Instructions:

35% lw
15% sw
30% add/nand
20% beq

5 ns – Register Read/Write
10 ns – ALU Operations
20 ns – Memory Access

What is the total execution time? (No Hazards)

Single Cycle: 100 * 60 = 6000 ns

Multi-Cycle: 20 * (35*5 + 15*4 + 30*4 + 20*4) = 8700 ns

Pipelined:

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Multi-Cycle Datapath

Timing Example

100 Instructions:

35% lw
15% sw
30% add/nand
20% beq

5 ns – Register Read/Write
10 ns – ALU Operations
20 ns – Memory Access

What is the total execution time? (No Hazards)

Single Cycle: 100 * 60 = 6000 ns

Multi-Cycle: 20 * (35*5 + 15*4 + 30*4 + 20*4) = 8700 ns

Pipelined: 20 * (4 + 100) = 2080 ns

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Data Hazards

Key Concepts

In what stage is data read from registers?

In what stage is data written to registers?

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Data Hazards

Key Concepts

In what stage is data read from registers?

Decode

In what stage is data written to registers?

Writeback

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Data Hazards

The Problem:

```
x = 5*y+3;
```

```
LDR R1 [R0, #wherever y is]
MUL R2 R1 #5
ADD R2 R2 #3
STR R2 [R0, #wherever x is]
```

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Data Hazards

Solutions:

- Avoidance
- Detect and Stall
- Detect and Forward

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Data Hazards

Pipeline Example

```
add  1  2  3
nand 3  5  6
lw   0  3  26
add  6  2  4
nand 4  3  1
```

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Exam Results

- Answer Keys are posted online
- Exams will be returned now ne  ek
- Regrade Requests:
  - Submit Scantron + written statement to IA/GSI/Professor
  - Before Friday