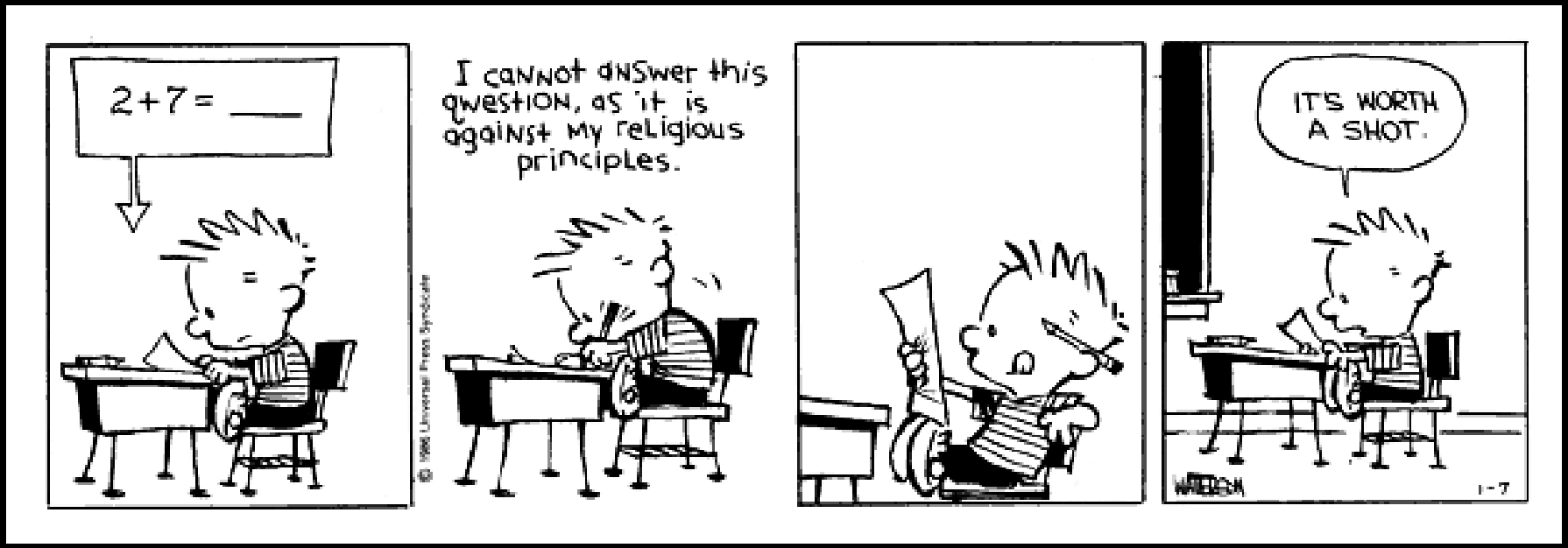
EECS 370 Discussion



Calvin and Hobbes
by Bill Watterson

EECS 370 Discussion

Exam

7:00 – 8:30 Tuesday (Tomorrow!)

Bring:

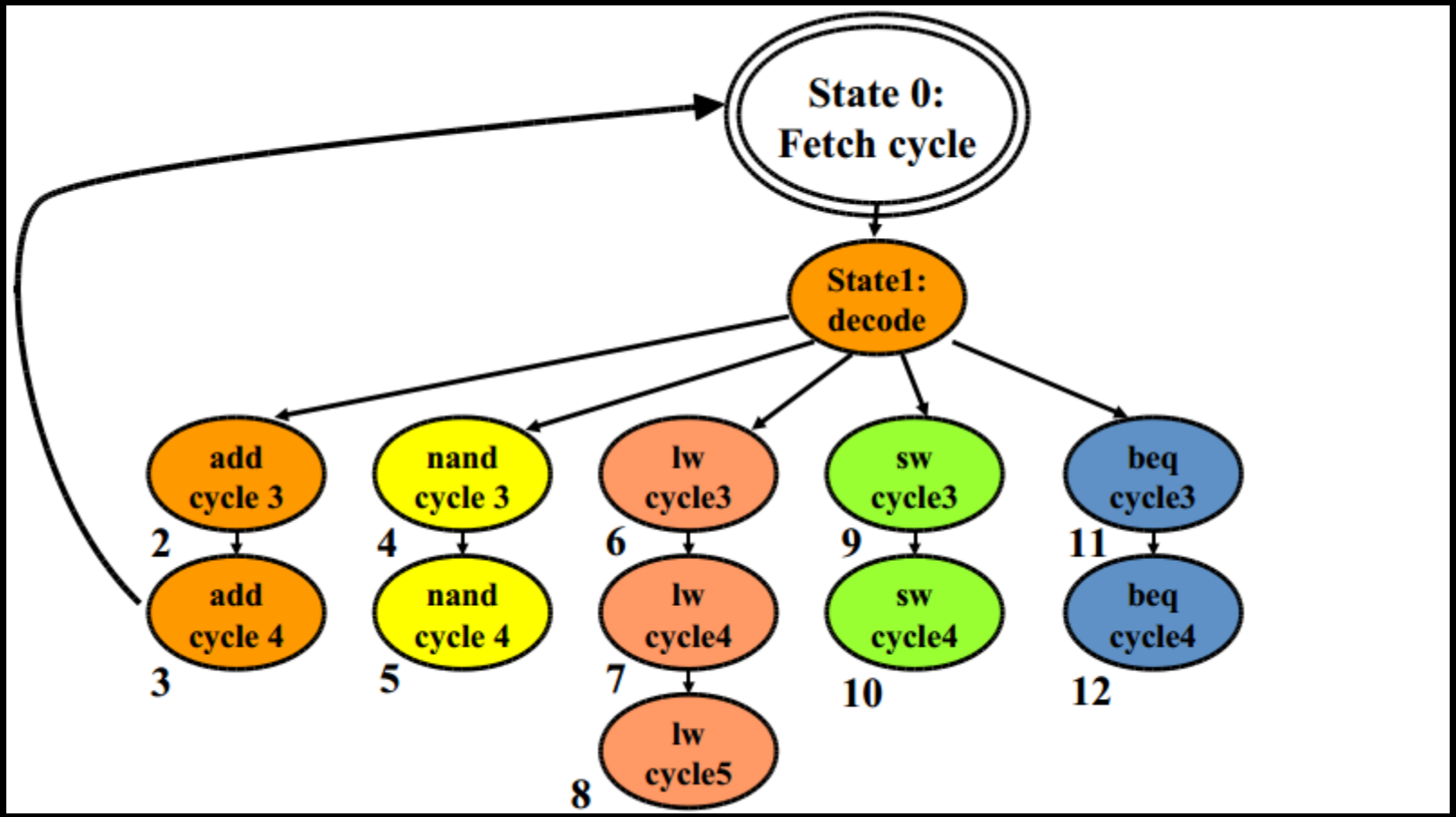
- Pencil
- Calculator
- Notes Sheet
  - letter-sized, double sided, 1 sheet

EECS 370 Discussion

- Exam Review
  - Multi-cycle Datapath
  - Pipeline Datapath
    - Hazards!
  - Caches

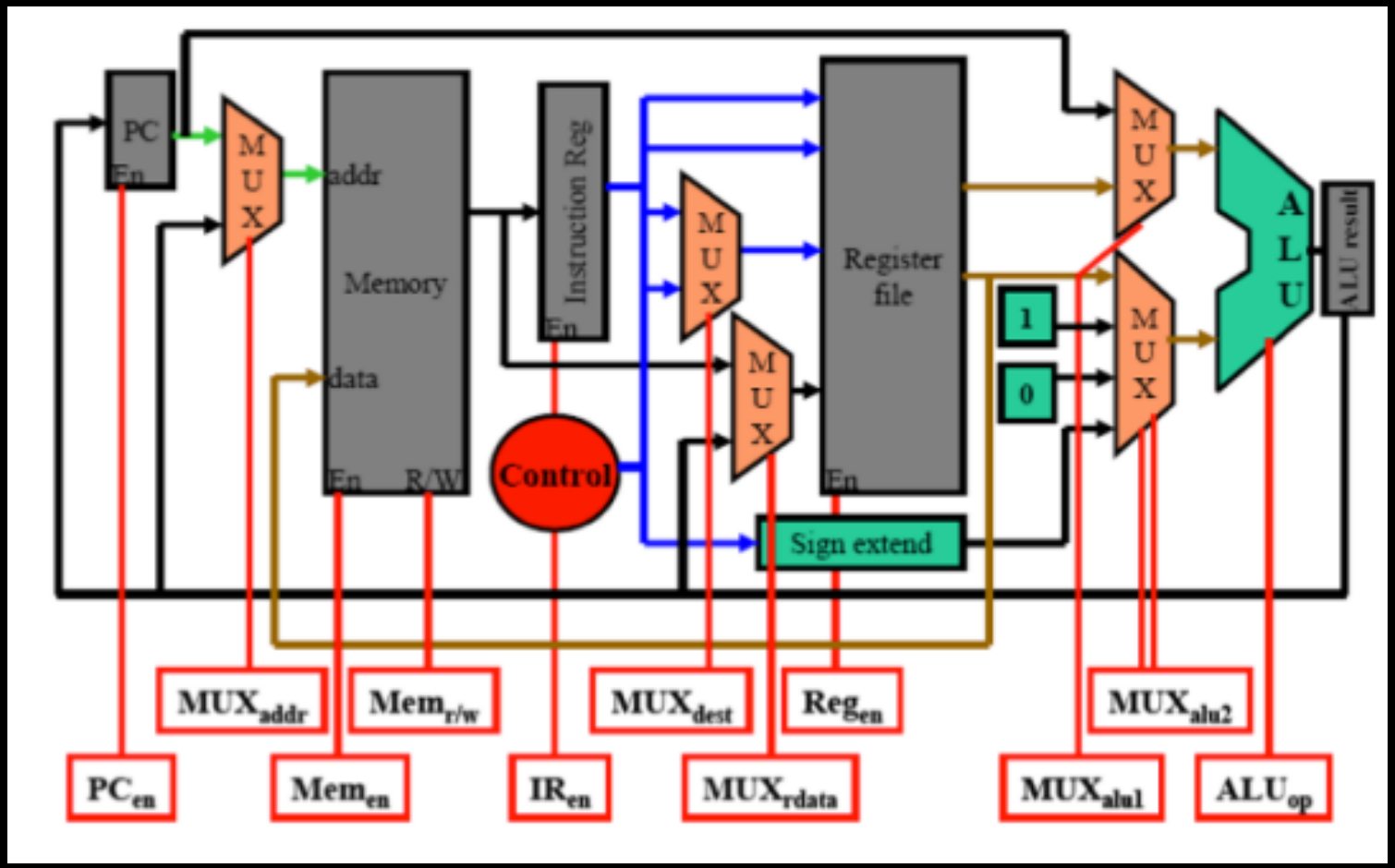
EECS 370 Discussion

Multi-Cycle Datapath



EECS 370 Discussion

Multi-Cycle Datapath



EECS 370 Discussion

Multi-Cycle Datapath

Frequency as compared to single-cycle?

Do all instructions take the same amount of time?

What is the CPI for a multi-cycle machine?

EECS 370 Discussion

Multi-Cycle Datapath

Frequency as compared to single-cycle?

Higher

Do all instructions take the same amount of time?

No! (ADD, NAND, SW, BEQ: 4 cycles, LW: 5 cycles)

What is the CPI for a multi-cycle machine?

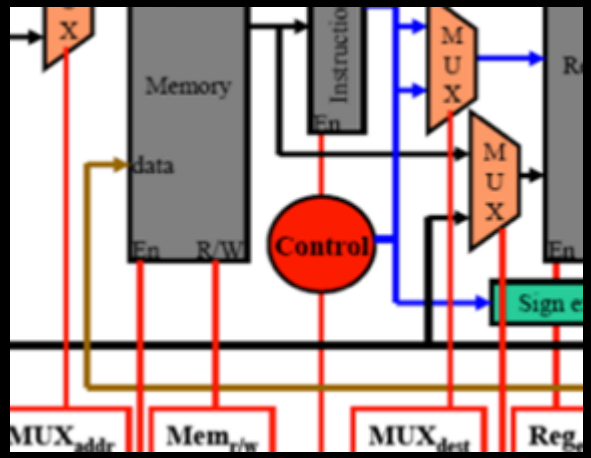
Depends on the instructions you run through it

EECS 370 Discussion

Multi-Cycle Datapath

Why doesn't multi-cycle have data hazards or control hazards?

What does the red Control circle on the diagram do?



EECS 370 Discussion

Multi-Cycle Datapath

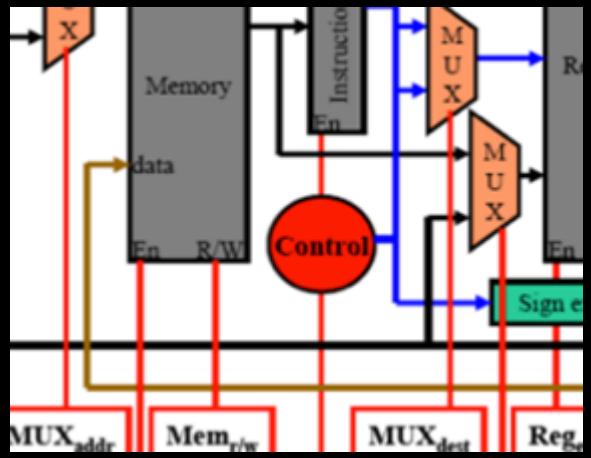
Why doesn't multi-cycle have data hazards or control hazards?

Only one instruction is running at a time

What does the red Control circle on the diagram do?

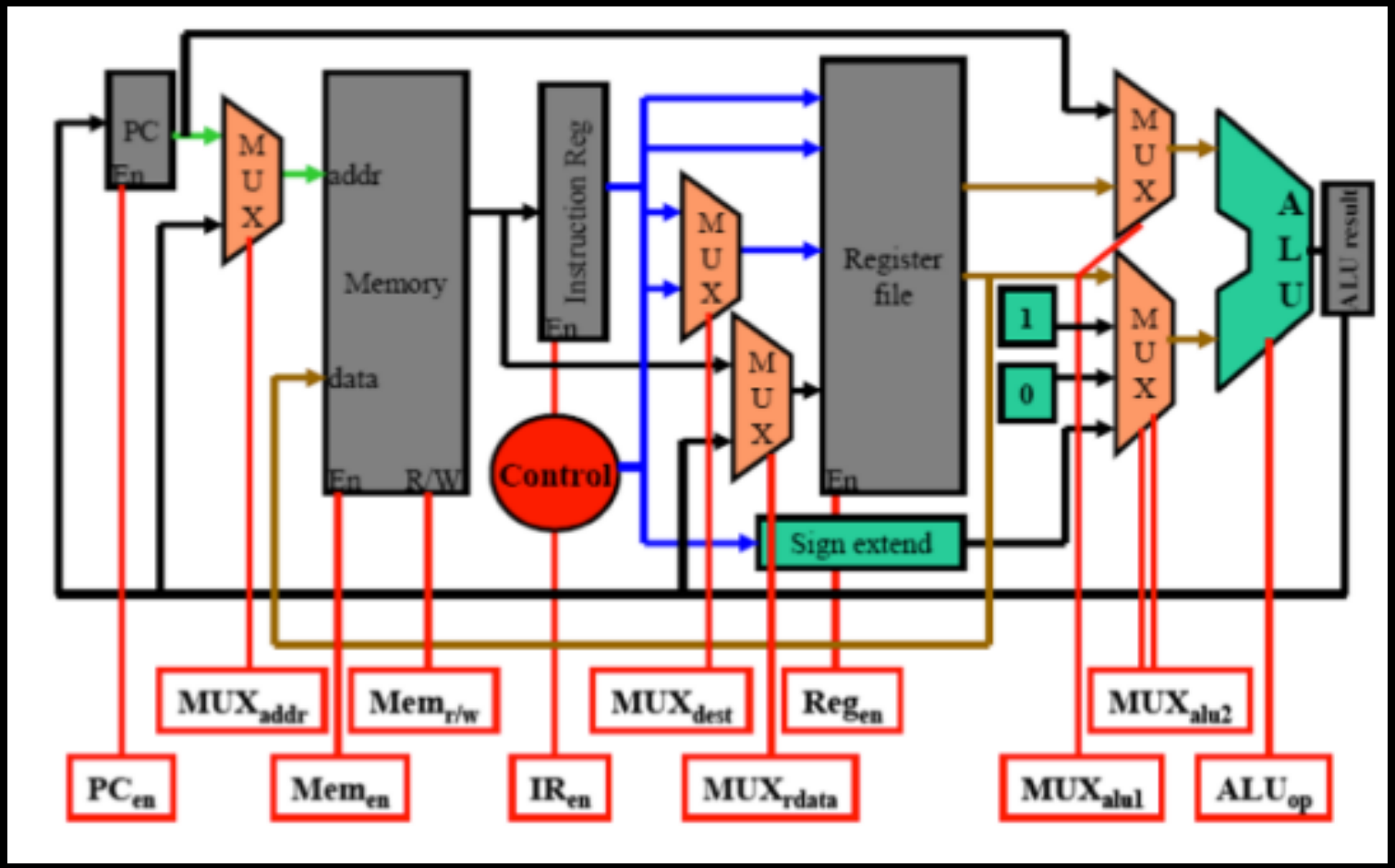
Sets the control signals for

muxes, ALU, Memory, and Reg



EECS 370 Discussion

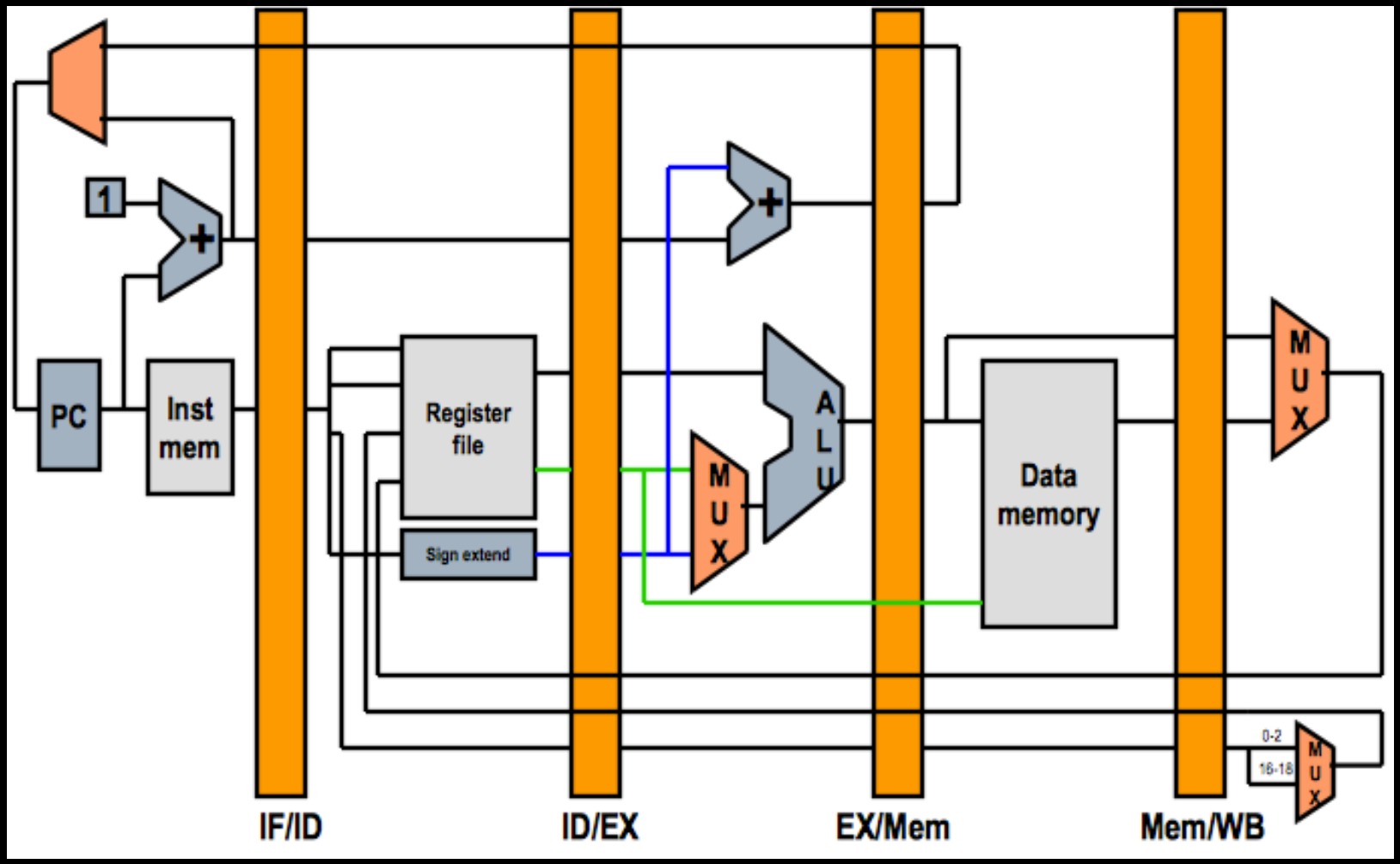
Multi-Cycle Datapath



Let's run an instruction through the datapath

EECS 370 Discussion

Pipeline Datapath



EECS 370 Discussion

Pipeline Datapath

Frequency as compared to single-cycle?

Do all instructions take the same amount of time?

What is the CPI for a pipelined processor?

EECS 370 Discussion

Pipeline Datapath

Frequency as compared to single-cycle?

Higher

Do all instructions take the same amount of time?

Yes

What is the CPI for a pipelined processor?

1 (over many instructions)

EECS 370 Discussion

Pipeline Datapath

Timing Example

1000 Instructions:

25% lw
5% sw
50% add/nand
20% beq

6 ns – Register Read/Write
2 ns – ALU Operations
10 ns – Memory Access

What is the total execution time? (No Hazards)

EECS 370 Discussion

Pipeline Datapath

Timing Example

1000 Instructions:

25% lw
5% sw
50% add/nand
20% beq

6 ns – Register Read/Write
2 ns – ALU Operations
10 ns – Memory Access

What is the total execution time? (No Hazards)

10 * (4+1000) = 10040 ns

EECS 370 Discussion

Data Hazards

Avoidance

Detect and Stall

Detect and Forward

EECS 370 Discussion

Pipeline Datapath

Timing Example

1000 Instructions:

25% lw
5% sw
50% add/nand
20% beq

6 ns – Register Read/Write
2 ns – ALU Operations
10 ns – Memory Access

37% of ADD/NAND instructions followed by dependent instruction

Detect and forward

What is the total execution time?

EECS 370 Discussion

Pipeline Datapath

Timing Example

1000 Instructions:

25% lw
5% sw
50% add/nand
20% beq

6 ns – Register Read/Write
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10 ns – Memory Access

37% of ADD/NAND instructions followed by dependent instruction

Detect and forward

What is the total execution time?

10 * (4+1000) = 10040 ns

EECS 370 Discussion

Control Hazards

No Branches

Avoid

Detect-and-stall

Speculate-and-squash

EECS 370 Discussion

Control Hazards

In a 27 stage pipeline, if Branches are resolved in Stage 14:

Which stages must be squashed?

EECS 370 Discussion

Control Hazards

In a 27 stage pipeline, if Branches are resolved in Stage 14:
Which stages must be squashed?

Stages 1 through 13

EECS 370 Discussion

Pipeline Datapath

Timing Example

1000 Instructions:

25% lw
5% sw
50% add/nand
20% beq

6 ns – Register Read/Write
2 ns – ALU Operations
10 ns – Memory Access

10% of BEQ instructions are mispredicted

Speculate-and-squash

What is the total execution time?

EECS 370 Discussion

Pipeline Datapath

Timing Example

1000 Instructions:

25% lw
5% sw
50% add/nand
20% beq

6 ns – Register Read/Write
2 ns – ALU Operations
10 ns – Memory Access

10% of BEQ instructions are mispredicted

Speculate-and-squash

What is the total execution time?

10 * (4+1000 + 1000*0.2*0.1*3) = 10640 ns

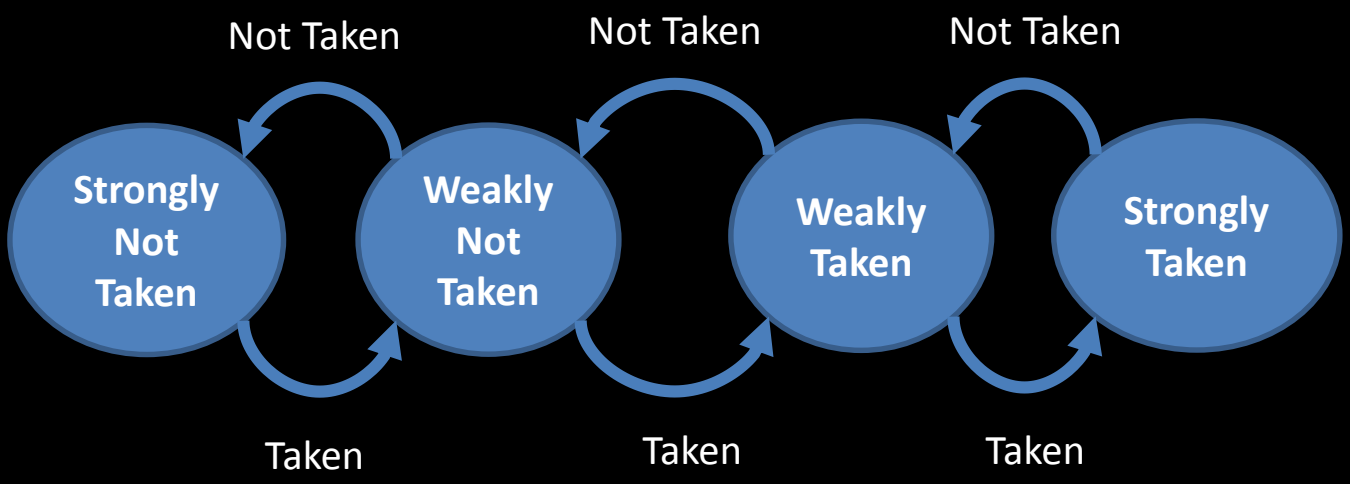
EECS 370 Discussion

Branch Predictors

Pattern is:

N N N T (Starting at Strongly Taken)

What is the mispredict rate?



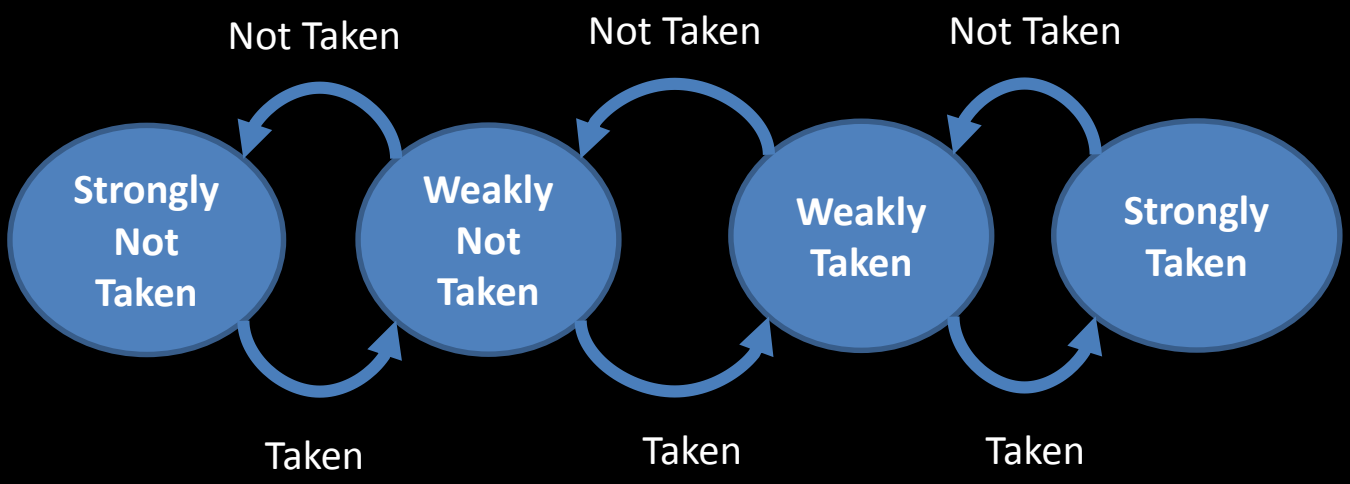
EECS 370 Discussion

Branch Predictors

Pattern is:

N N N T (Starting at Strongly Taken)

What is the mispredict rate? 25%



EECS 370 Discussion

Caches

What are the types of Locality?

What's the calculation for Block Index bits?

What's the calculation for Set Index bits?

EECS 370 Discussion

Caches

What are the types of Locality?

Spatial & Temporal

What's the calculation for Block Index bits?

$\log_2$(block size)

What's the calculation for Set Index bits?

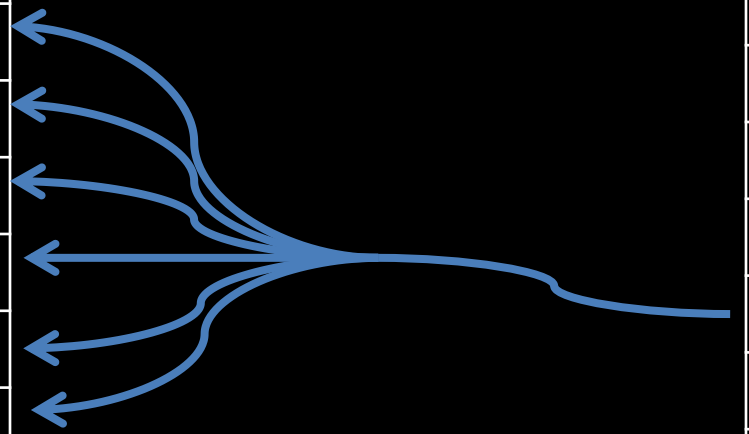
$\log_2$(number of sets)

EECS 370 Discussion

Types of Caches

Fully Associative

Cache	
Tag	Data



Memory	
0x1000	10
0x1004	20
0x1008	30
0x100C	40
0x1010	50
0x1014	60
0x1018	70
0x101C	80
0x1020	90
0x1024	100
0x1028	110

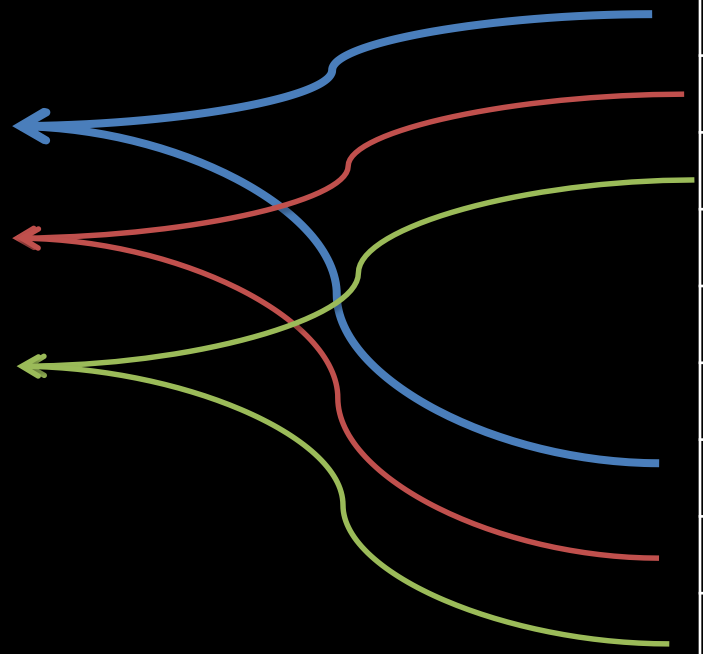
Blocks map to any cache line

EECS 370 Discussion

Types of Caches

Direct Mapped

Cache	
Tag	Data



Memory	
0x1000	10
0x1004	20
0x1008	30
0x100C	40
0x1010	50
0x1014	60
0x1018	70
0x101C	80
0x1020	90
0x1024	100
0x1028	110

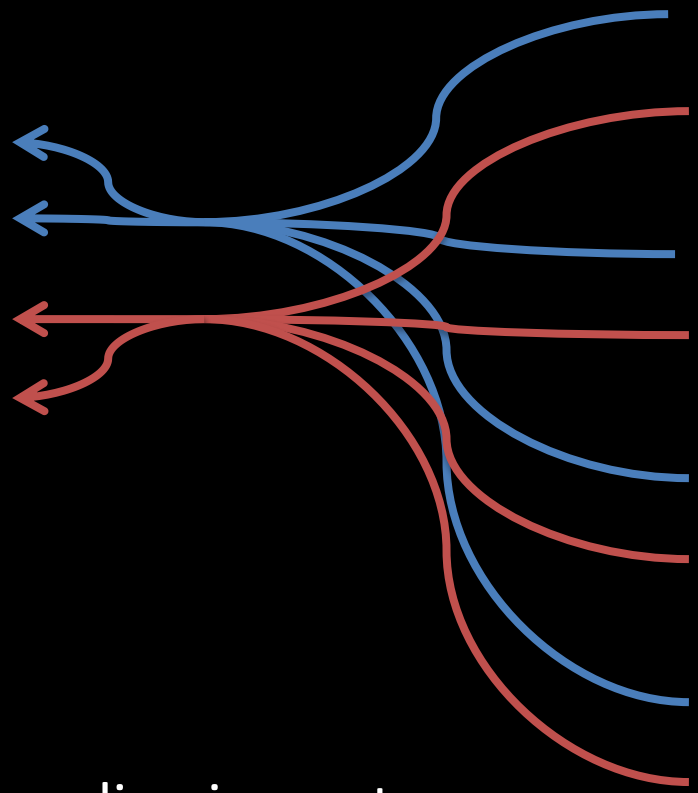
Blocks map to one cache line

EECS 370 Discussion

Types of Caches

Set Associative

Cache	
Tag	Data



Memory	
0x1000	10
0x1004	20
0x1008	30
0x100C	40
0x1010	50
0x1014	60
0x1018	70
0x101C	80
0x1020	90
0x1024	100
0x1028	110

Blocks map to any line in a set

EECS 370 Discussion

Caches

What are the Three C's and how do we determine them?

EECS 370 Discussion

Caches

What are the Three C's and how do we determine them?

Compulsory – if we have never loaded it

Capacity – misses in same size fully associative cache

Conflict – any additional misses in actual cache

EECS 370 Discussion

Caches

What's the difference between Write Allocate and No Write Allocate?

What's the difference between Write Through and Write Back?

EECS 370 Discussion

Caches

What's the difference between Write Allocate and No Write Allocate?

- Write Allocate – add to cache on write miss
- No Write Allocate – don't add to cache

What's the difference between Write Through and Write Back?

- Write Through – always write to memory
- Write Back – just write to cache

EECS 370 Discussion

Caches

Timing Example

1000 Instructions:

25% lw
5% sw
50% add/nand
20% beq

6 ns – Register Read/Write
2 ns – ALU Operations
10 ns – Memory Access

10% of BEQ instructions are mispredicted, Speculate-and-squash

20% of all memory accesses miss caches. Misses take 20 cycles

What is the total execution time?

EECS 370 Discussion

Caches

Timing Example

1000 Instructions:

25% lw
5% sw
50% add/nand
20% beq

6 ns – Register Read/Write
2 ns – ALU Operations
10 ns – Memory Access

10% of BEQ instructions are mispredicted, Speculate-and-squash

20% of all memory accesses miss caches. Misses take 20 cycles

What is the total execution time?

10 * (4+1000 + 1000*0.2*0.1*3)

+ 10 * (1000*.2*20 + 1000*.25*.2*20 +1000*.05*.2*20)

= 62640 ns