

EECS 370 Discussion

THERE'S BEEN A LOT OF CONFUSION OVER 1024 vs 1000, KBYTE vs KBIT, AND THE CAPITALIZATION FOR EACH.

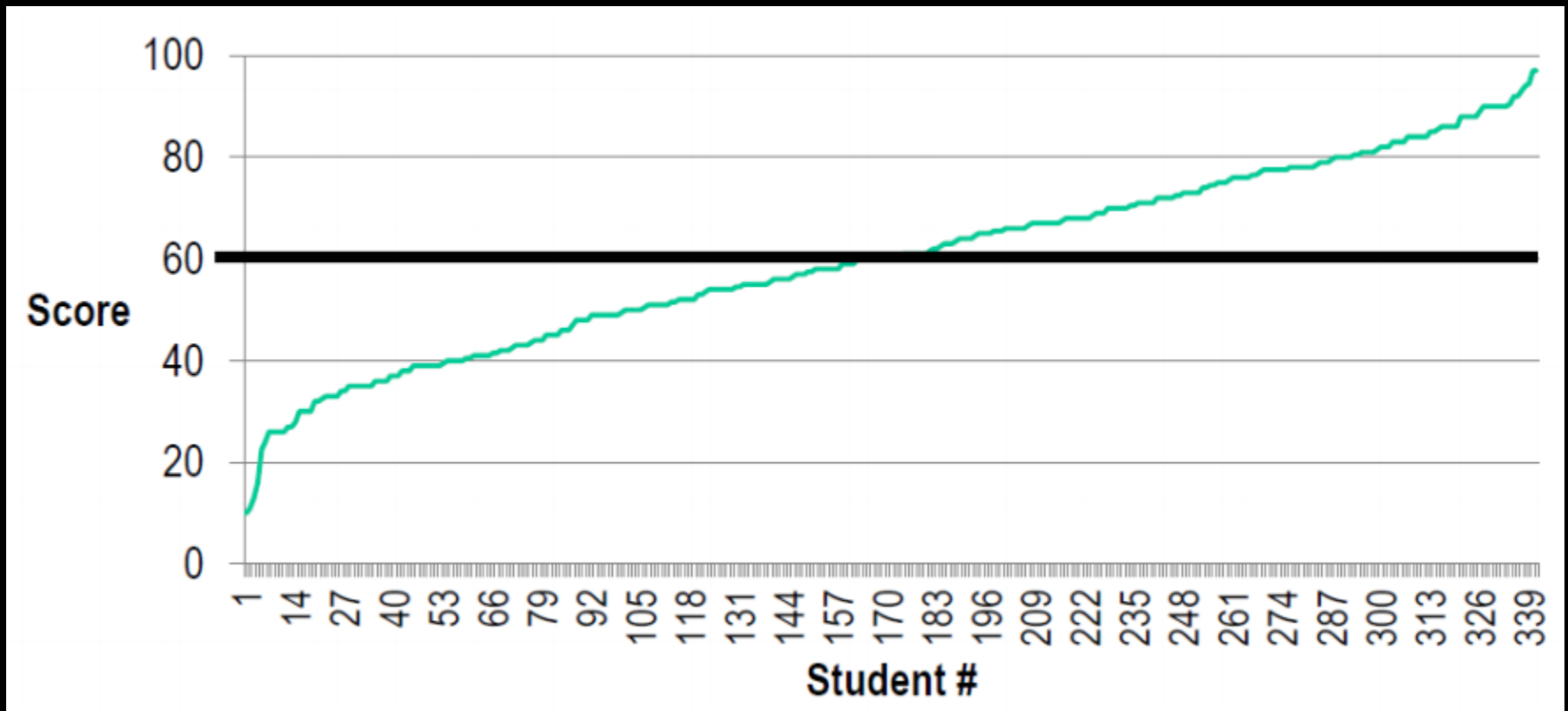
HERE, AT LAST, IS A SINGLE, DEFINITIVE STANDARD:

SYMBOL	NAME	SIZE	NOTES
kB	KILOBYTE	1024 BYTES <small>OR</small> 1000 BYTES	1000 BYTES DURING LEAP YEARS, 1024 OTHERWISE
KB	KELLY-BOOTLE STANDARD UNIT	1012 BYTES	COMPROMISE BETWEEN 1000 AND 1024 BYTES
KiB	IMAGINARY KILOBYTE	$1024\sqrt{2}$ BYTES	USED IN QUANTUM COMPUTING
kb	INTEL KILOBYTE	1023.937528 BYTES	CALCULATED ON PENTIUM F.P.U.
Kb	DRIVEMAKER'S KILOBYTE	CURRENTLY 908 BYTES	SHRINKS BY 4 BYTES EACH YEAR FOR MARKETING REASONS
KBa	BAKER'S KILOBYTE	1152 BYTES	9 BITS TO THE BYTE SINCE YOU'RE SUCH A GOOD CUSTOMER

xkcd

EECS 370 Discussion

Exam 2



High: 97 Low: 10 Average 60.4

EECS 370 Discussion

Roadmap to end of semester

- Project 4 – Friday 12/6 (Due tonight at 11:59 w/ 3 slip days)
- Homework 7 – Tuesday 12/7 (Tomorrow)
- Final Exam – Monday 12/16 10:30 am – 12:30 pm
make sure you don't have a conflict...

EECS 370 Discussion

- Virtual Memory
 - Physically Addressed & Virtually Addressed
 - Hierarchical Page Tables
- Hard Drives
 - Overview
 - Access Time
- General Review

EECS 370 Discussion

Virtual Memory

Concepts

Physical Addresses are in?

Virtual Addresses are in?

What does the TLB hold?

EECS 370 Discussion

Virtual Memory

Concepts

Physical Addresses are in?

Hardware

Virtual Addresses are in?

Software

What does the TLB hold?

Physical Page Numbers

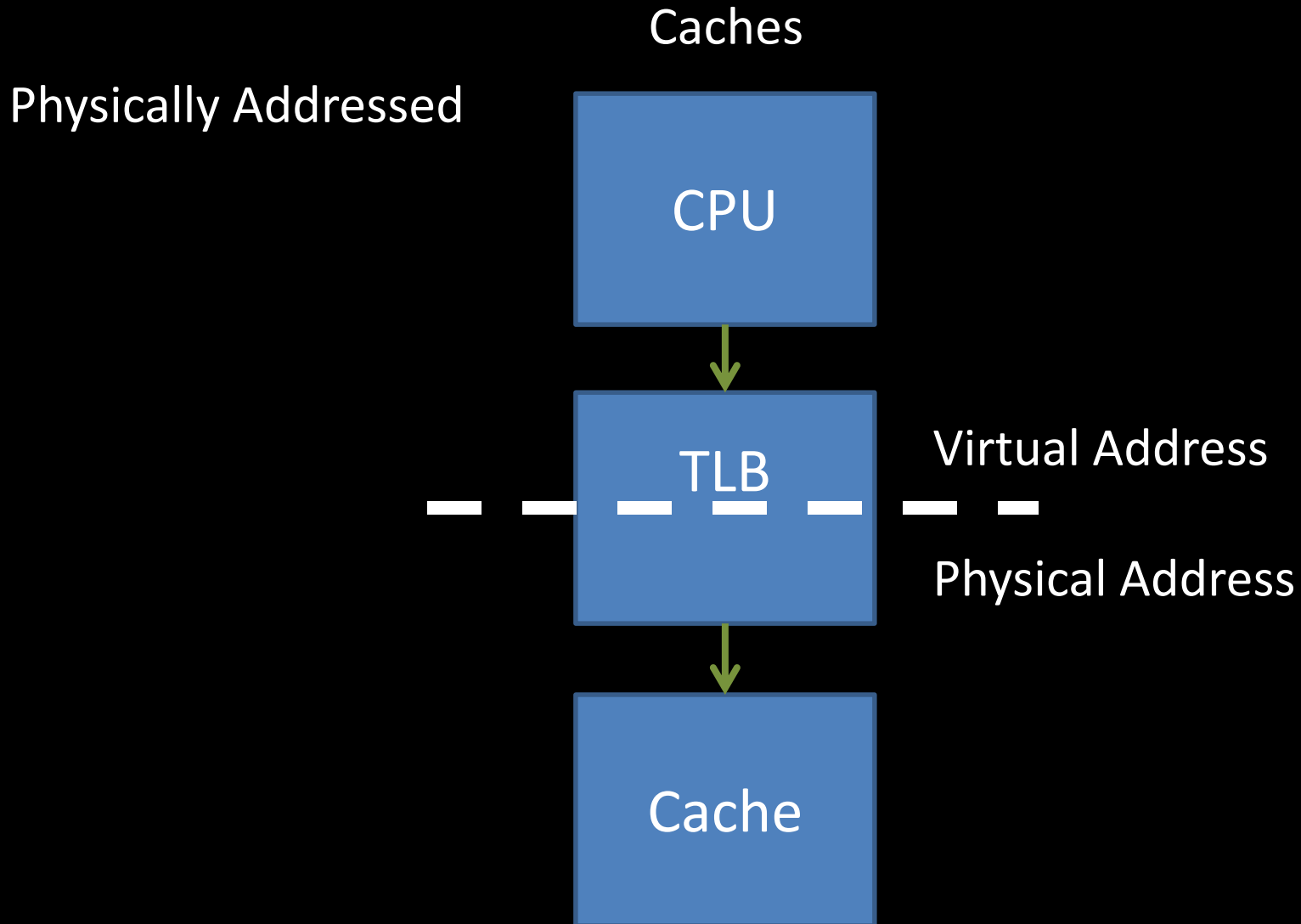
EECS 370 Discussion

Caches

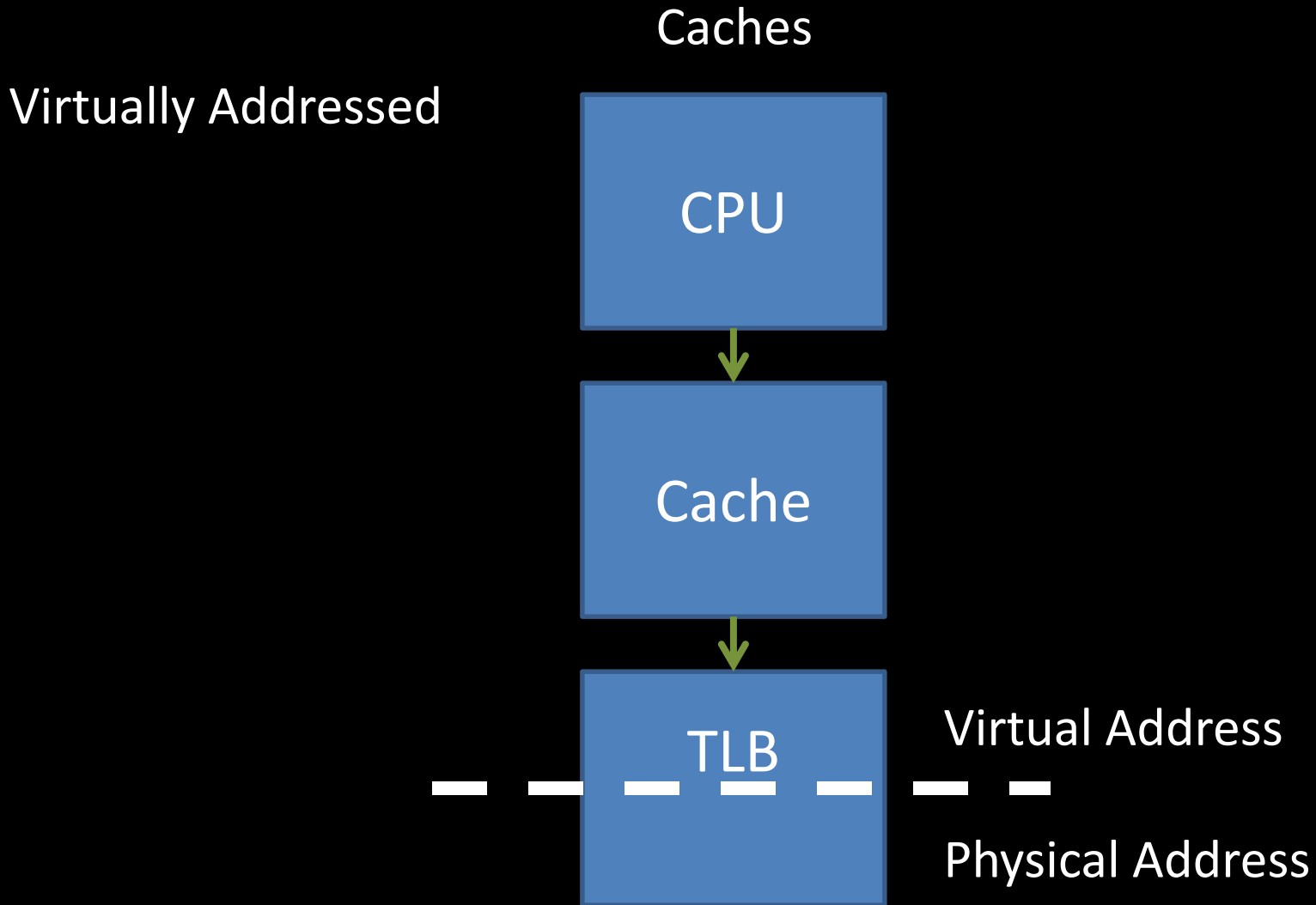
Problem:

Where do we put the cache in a VM system?

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EECS 370 Discussion



EECS 370 Discussion

Caches

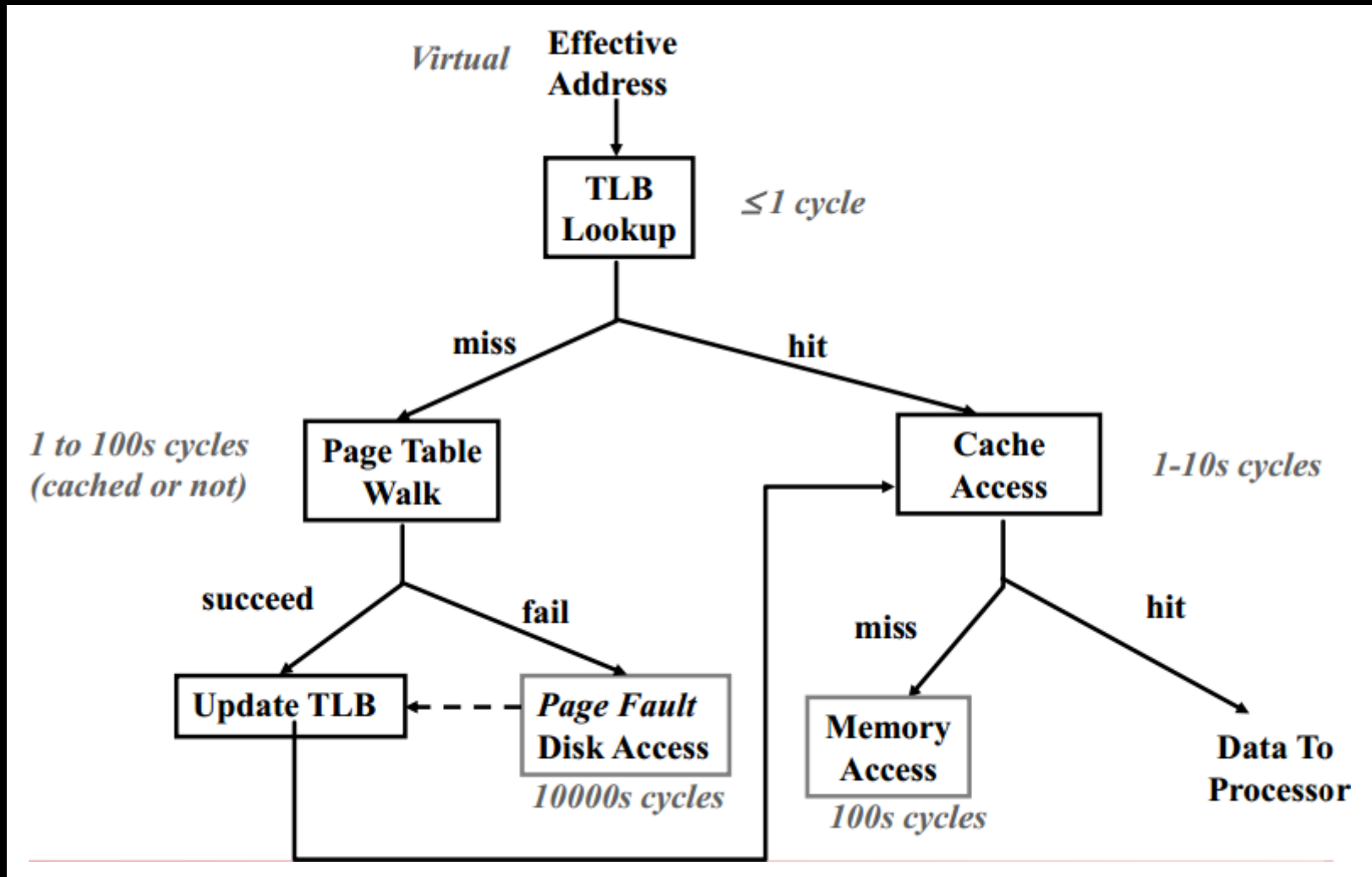
Performance Problem

	Hit Rate	Access Time
TLB	99%	1 cycle
Cache	90%	1 cycle
Main Memory	99.99%	100 cycles
Disk	100%	1,000,000 cycles

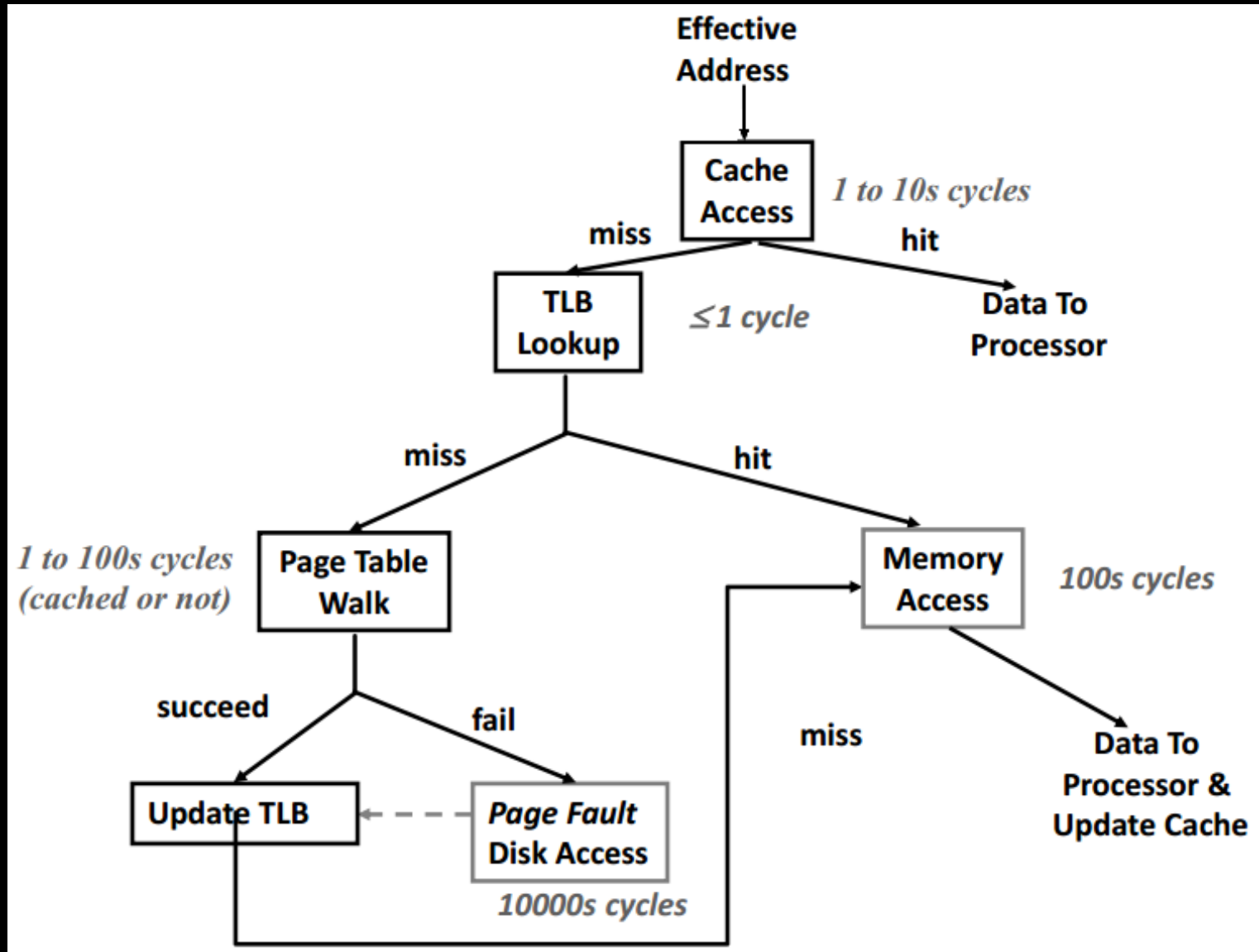
Find memory latency for virtually addressed and physically addressed systems.

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Caches



EECS 370 Discussion



EECS 370 Discussion

Hierarchical Page Tables

32-bit virtual addresses

Page Size: 8kB

Page Entry Size: 8B

How many levels of page tables must there be?

Where do each of the address bits go?

EECS 370 Discussion

Hierarchical Page Tables

32-bit virtual addresses

Page Size: 8kB

Page Entry Size: 8B

How many levels of page tables must there be?

2 levels

Where do each of the address bits go?

10-bit superpage table, 9-bit subpage table, 13-bit page offset

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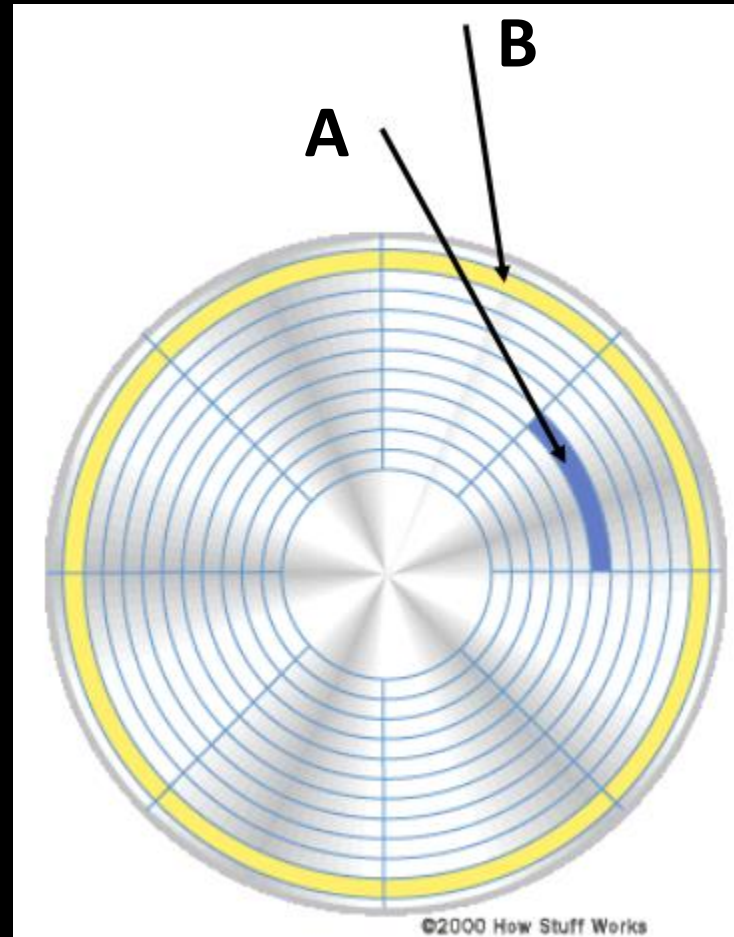
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Hard Drive Disk

Picture of one side of a platter

A - Sector

B - Track



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Hard Drive Disk

Access Time

- Seek Time – Moving to correct track
- Rotational Delay – Waiting for correct sector
- Transfer Time – Reading data from disk

- Wait Time & Controller Overhead – Additional delays

Is Random Access or Sequential Access better?

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Hard Drive Disk

Access Time

5400 RPM

2 kB Sectors

512 Sectors per Track

8 ms Seek Time

No overhead

What is the time to access one sector?

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Exam Review

There will be two exam review sessions

Thursday, 4-6 pm, Chrysler 220

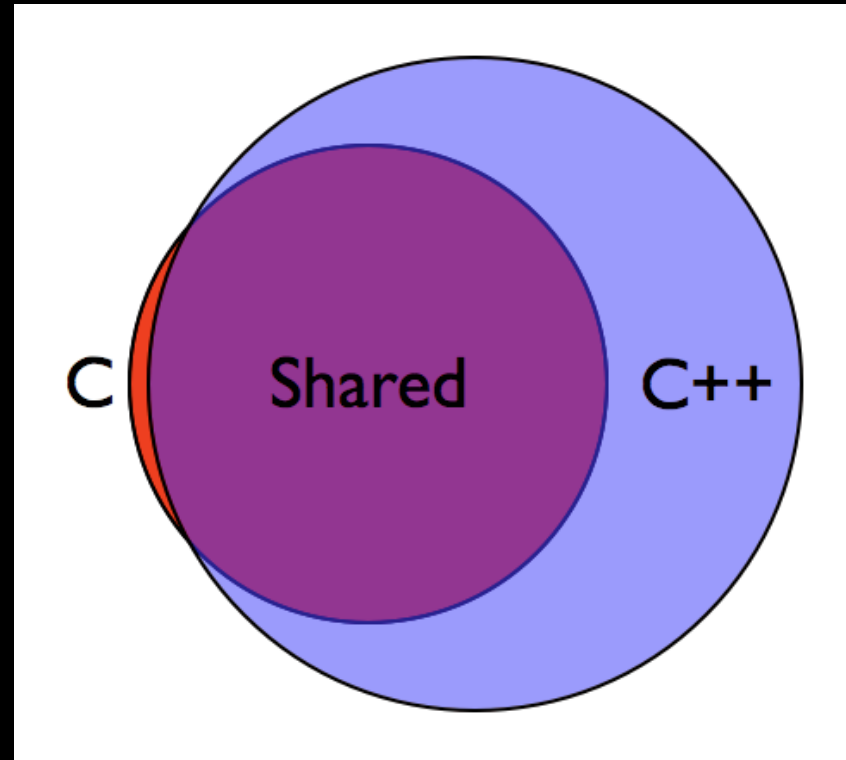
Sunday , 1-3 pm, Chrysler 220

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Exam Review

Discussion 1

- How does C work?
- LC2K Instructions

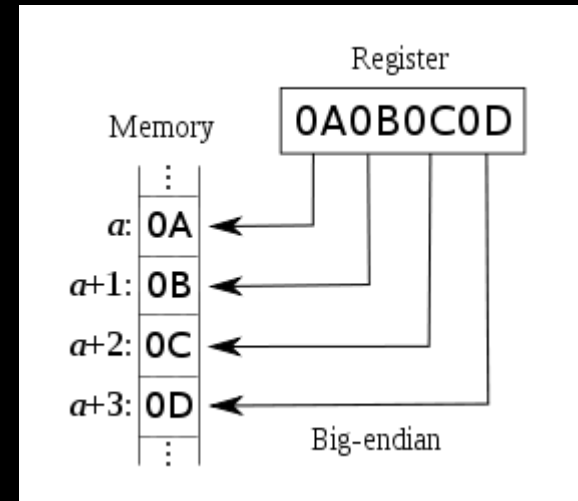


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Exam Review

Discussion 2

- ARM Addressing
- Struct Data Layout
- Conditional Assembly

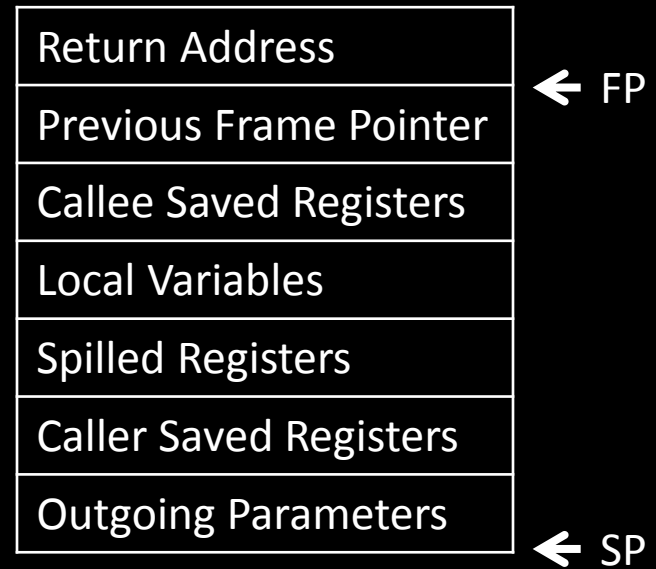


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Exam Review

Discussion 3

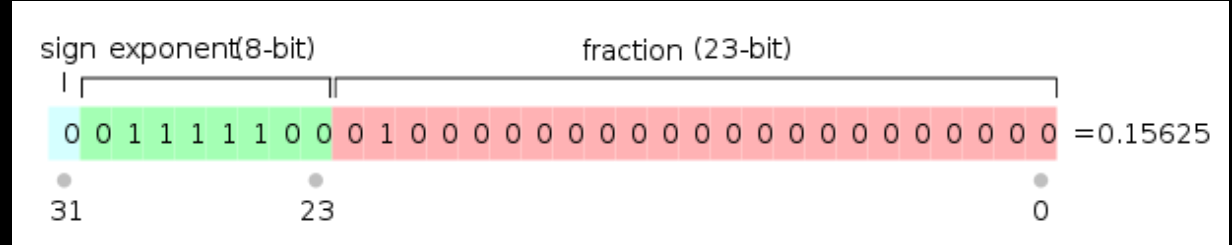
- Caller / Callee Saved Registers
- Memory Layout
- Linking & Object Files



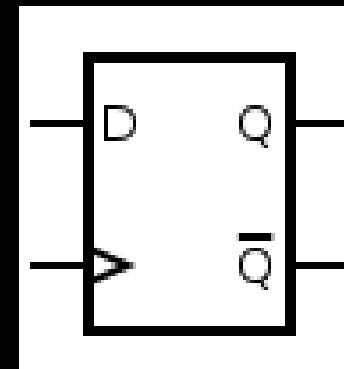
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Exam Review

Discussion 4



- Floating Point
- Finite State Machines
- Combinational Logic
- Sequential Logic



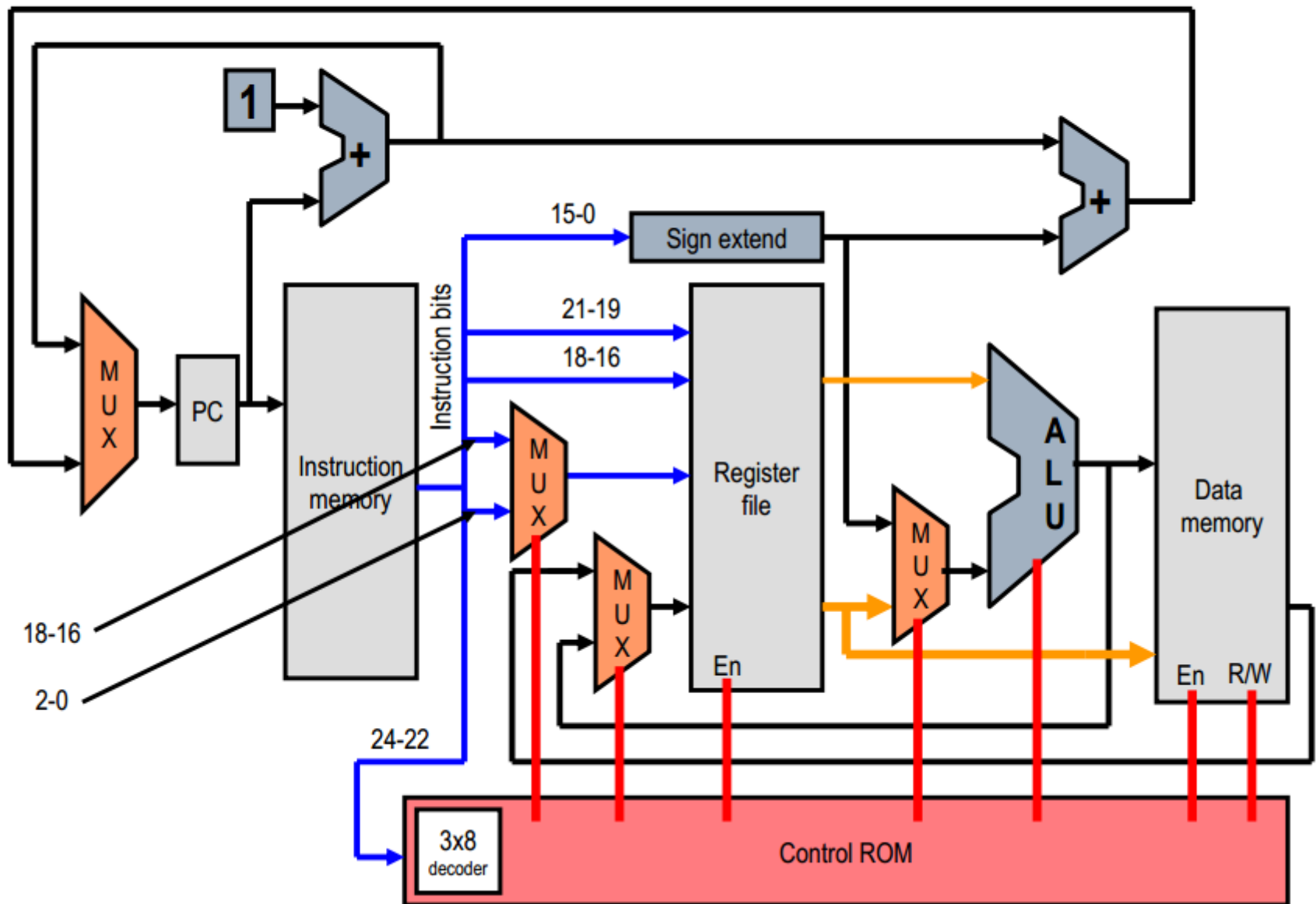
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Exam Review

Discussion 5

- Single Cycle Datapath

LC2Kx Datapath Implementation

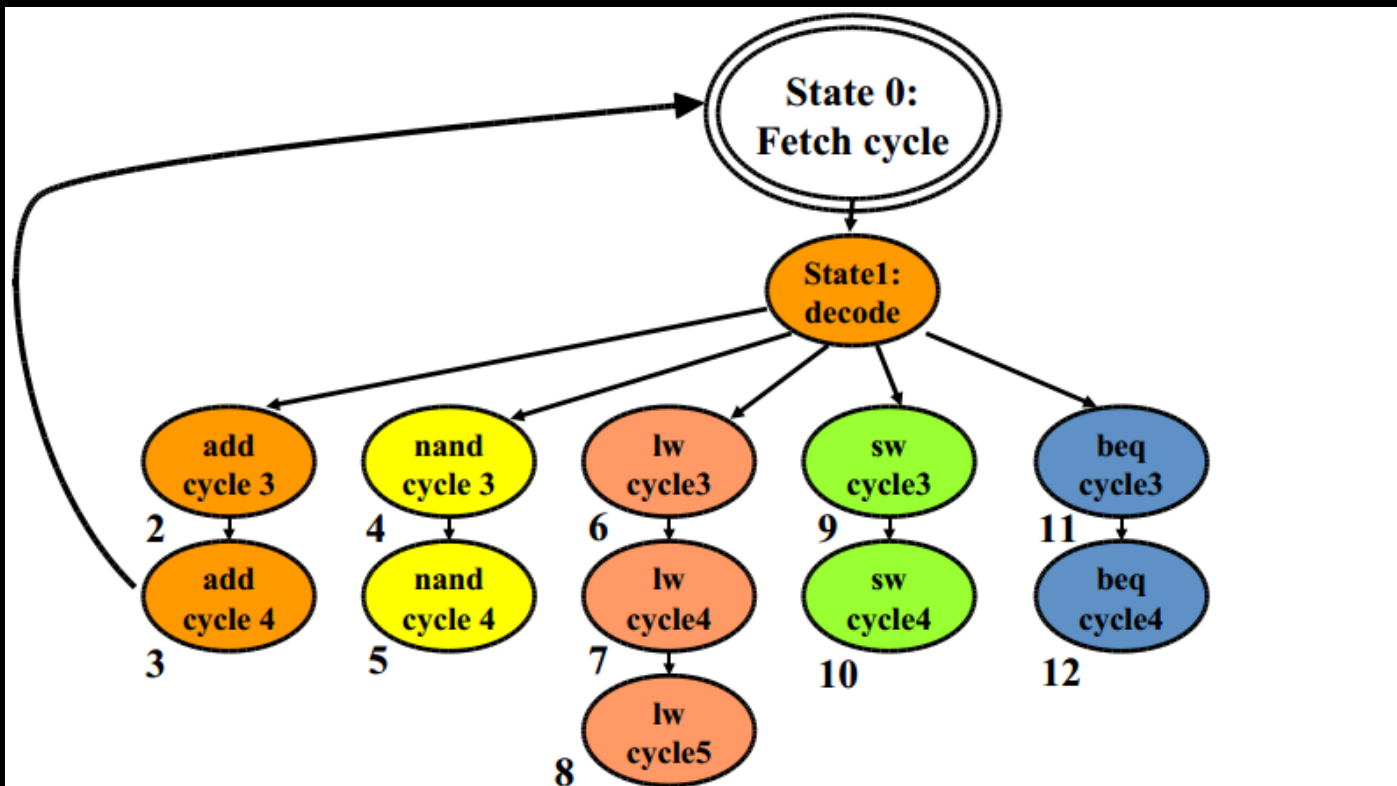


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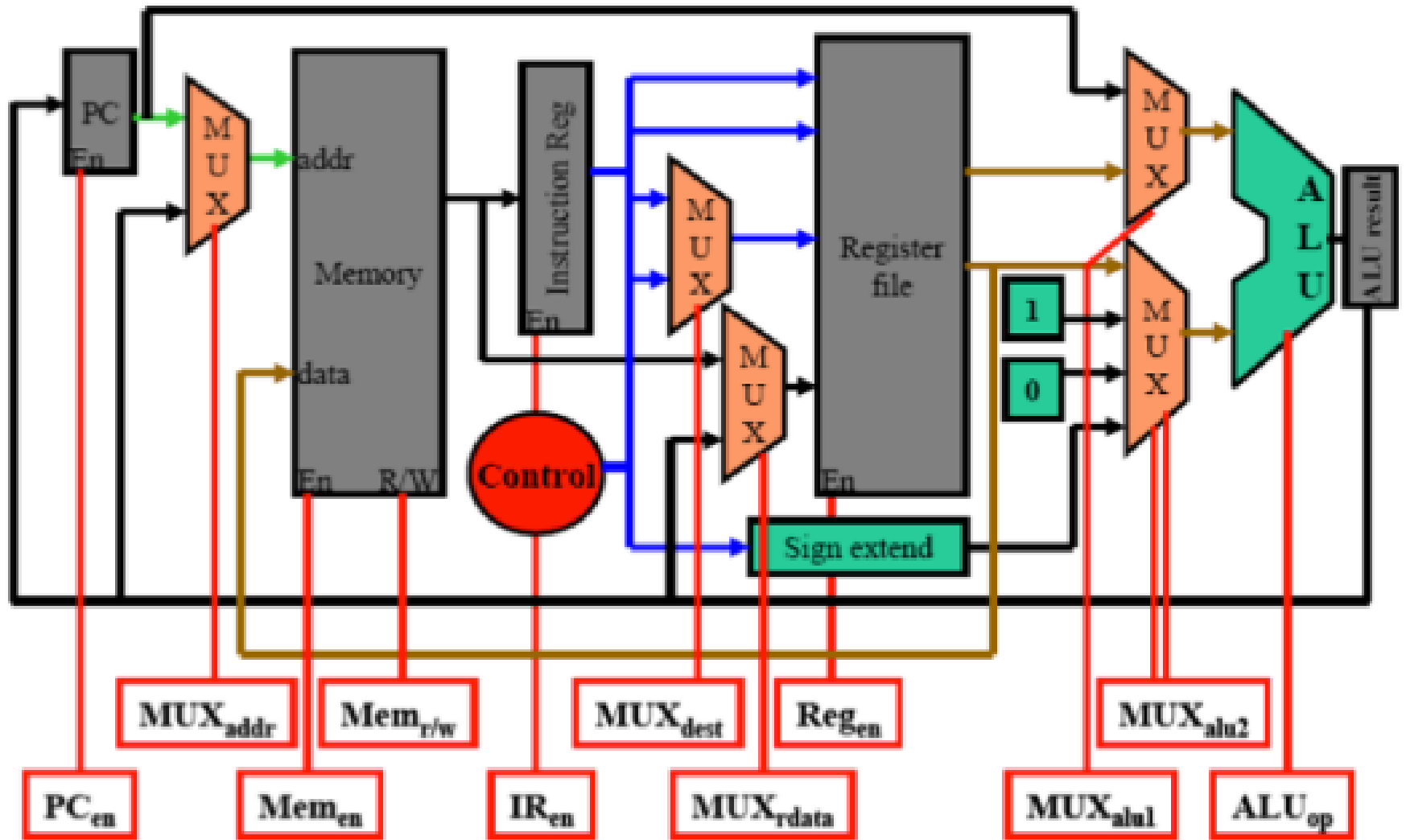
Exam Review

Discussion 6

- Multi Cycle Datapath



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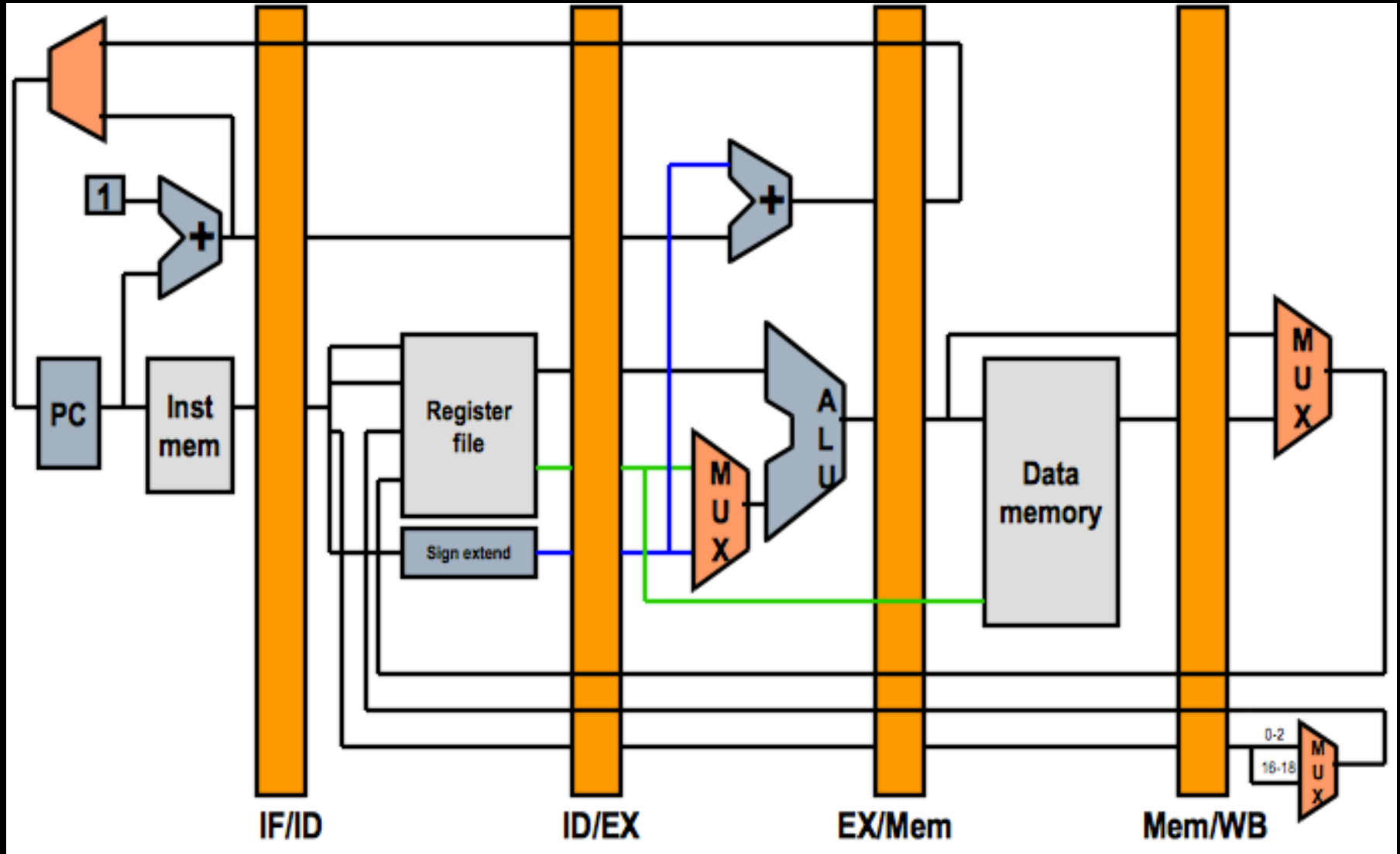
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Exam Review

Discussion 7

- Pipelined Processor
- Data Hazards

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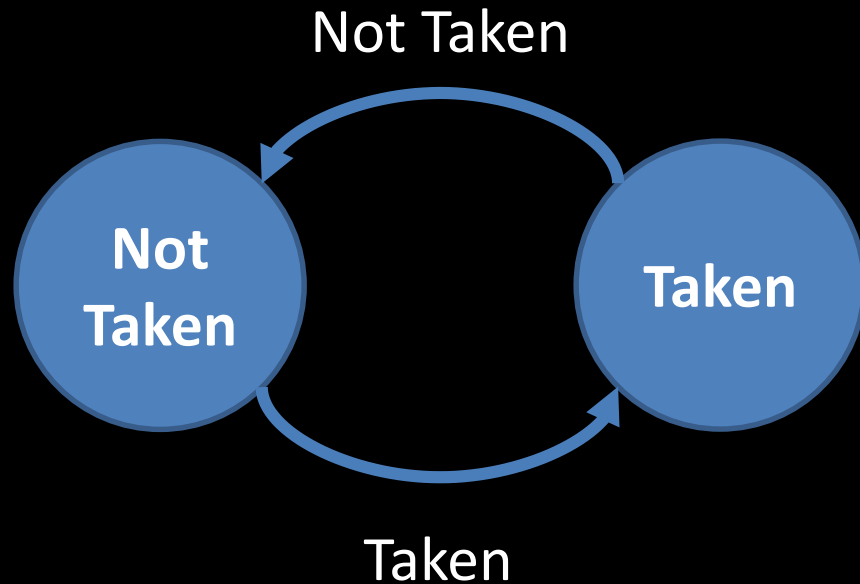


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Exam Review

Discussion 8

- Control Hazards
- Branch Prediction

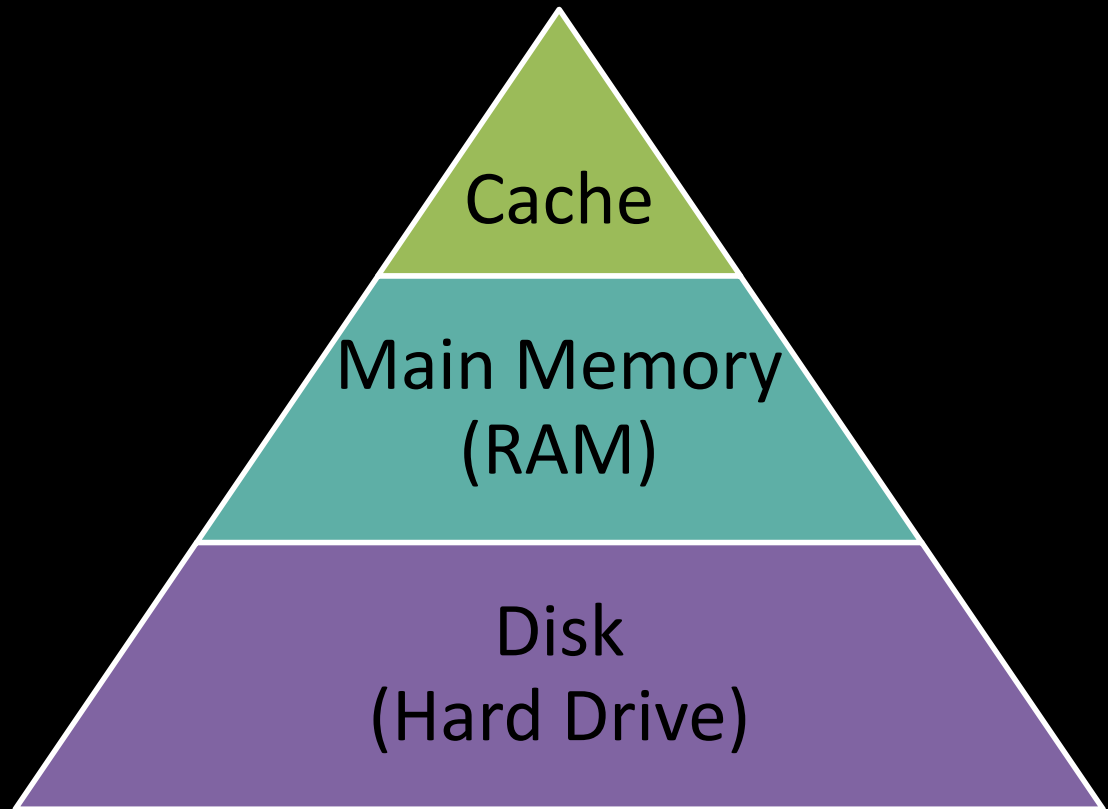


EECS 370 Discussion

Exam Review

Discussion 9

- Caches



EECS 370 Discussion

Exam Review

Discussion 10

- Exam Review

Discussion 11

- Virtual Memory

Discussion 12

- Virtual Memory
- Disks