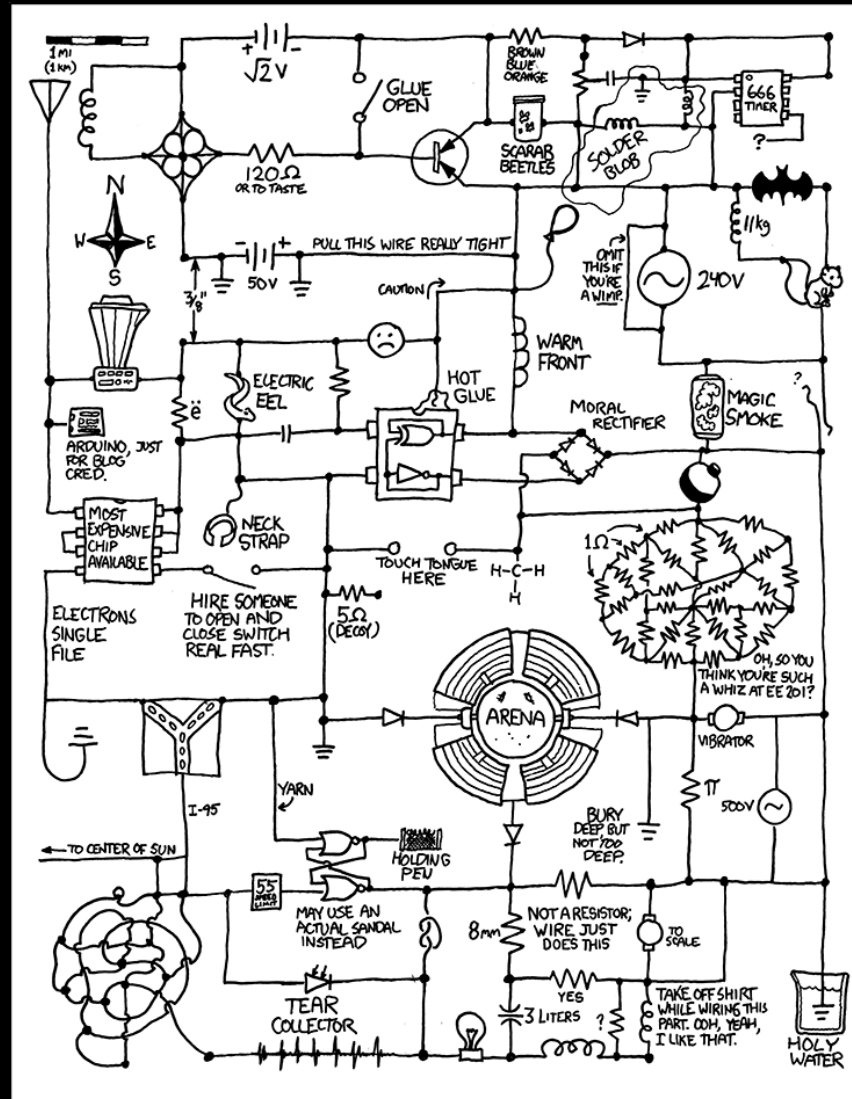


# EECS 370 Discussion



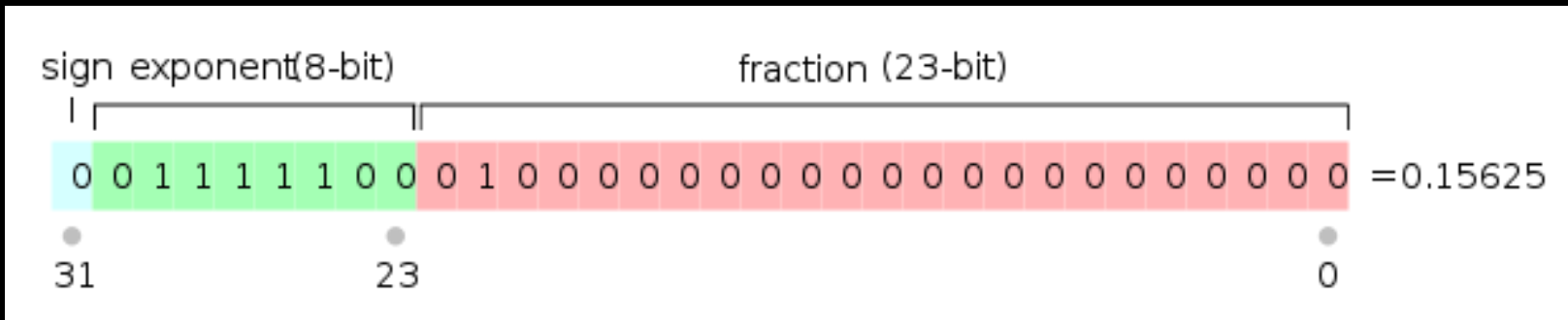
# EECS 370 Discussion

## Topics Today:

- Floating Point
- Finite State Machines
- Combinational Logic
- Sequential Logic

# EECS 370 Discussion

## Floating Point



Exponent

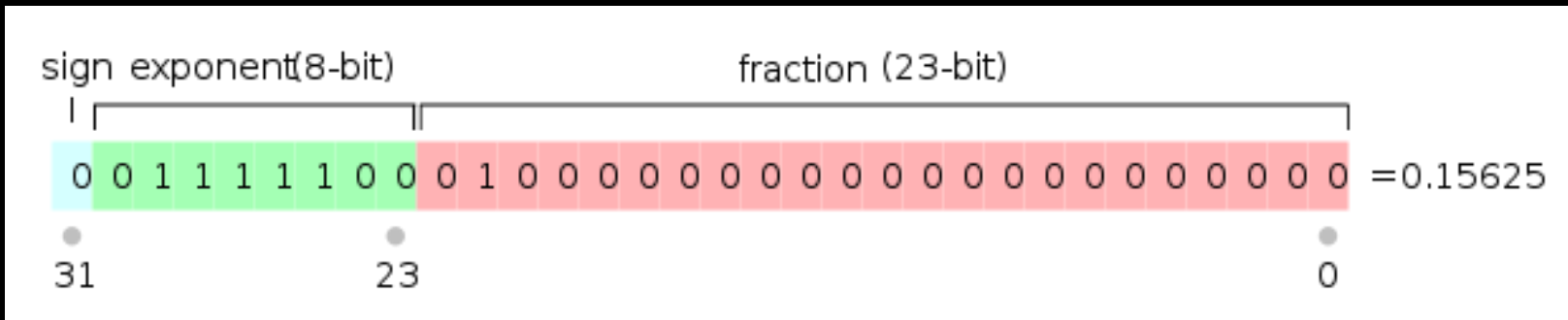
Biased by 127

Significand

Additional 1 before the decimal sign

# EECS 370 Discussion

## Floating Point



Don't forget about zero!

# EECS 370 Discussion

## Floating Point

Addition

$$-1.1011 \cdot (2^2) + 1.01 \cdot (2^0)$$

# EECS 370 Discussion

## Floating Point

Addition

$$-1.1011 \cdot (2^2) + 1.01 \cdot (2^0)$$

$$= -1.0110 \cdot (2^2)$$

# EECS 370 Discussion

## Floating Point

Addition

$$\begin{array}{rcl} -1.1011 \cdot (2^2) & + & 1.01 \cdot (2^0) \\ [-6.75] & & [1.25] \end{array}$$

$$\begin{array}{r} = -1.0110 \cdot (2^2) \\ [-5.5] \end{array}$$

# EECS 370 Discussion

## Floating Point

### Multiplication

$$\begin{array}{ccc} -1.1011 \cdot (2^2) & * & 1.01 \cdot (2^0) \\ [-6.75] & & [1.25] \end{array}$$



# EECS 370 Discussion

## Floating Point

### Multiplication

$$\begin{array}{rcl} -1.1011 \cdot (2^2) & * & 1.01 \cdot (2^0) \\ [-6.75] & & [1.25] \end{array}$$

$$= -1.0000111 \cdot (2^3)$$

# EECS 370 Discussion

## Floating Point

### Multiplication

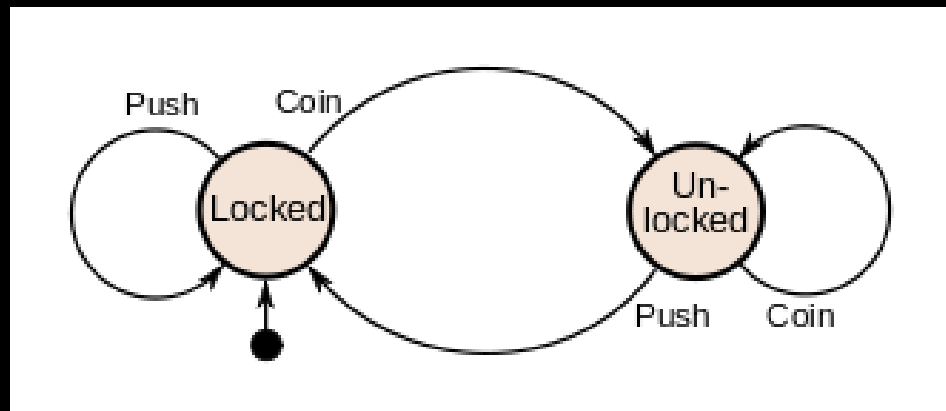
$$\begin{array}{rcl} -1.1011 \cdot (2^2) & * & 1.01 \cdot (2^0) \\ [-6.75] & & [1.25] \end{array}$$

$$\begin{array}{r} = -1.0000111 \cdot (2^3) \\ [-8.4375] \end{array}$$

# EECS 370 Discussion

## Finite State Machines

Diagram of State, Conditions to change state, and Outputs  
Conditions to change are based on inputs



# EECS 370 Discussion

## Finite State Machines

Example: Output a 1 on the pattern 001

States:

Pattern '1'

Pattern '0'

Pattern '00'

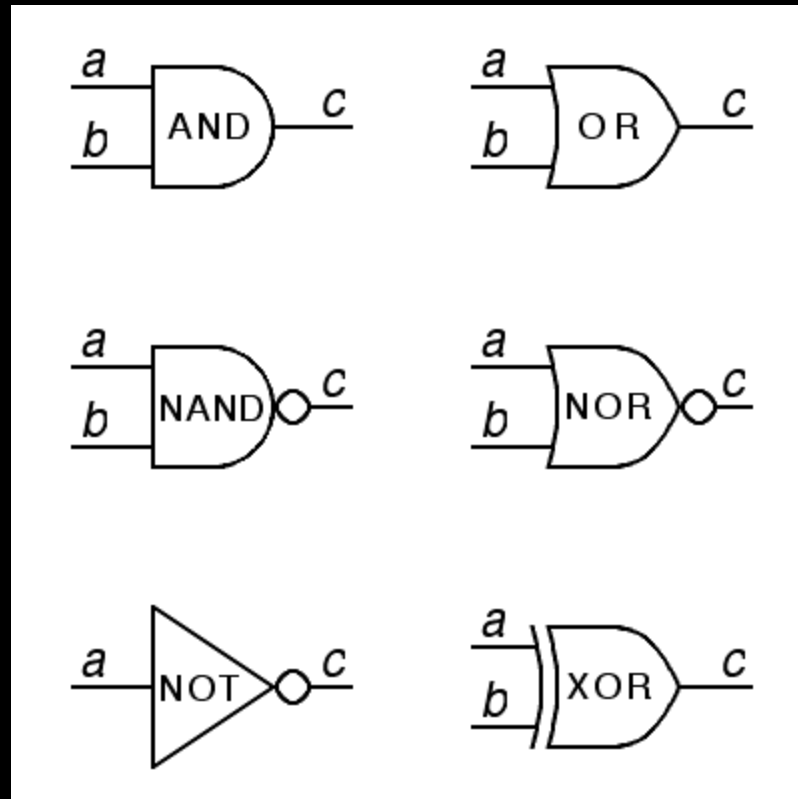
Pattern '001'    =>    Output = 1

# EECS 370 Discussion

## Combinational Logic

Digital circuit representing a Boolean equation

Truth tables!!

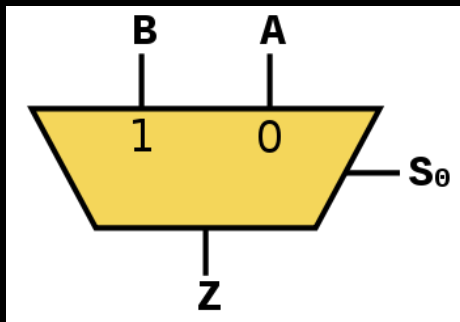
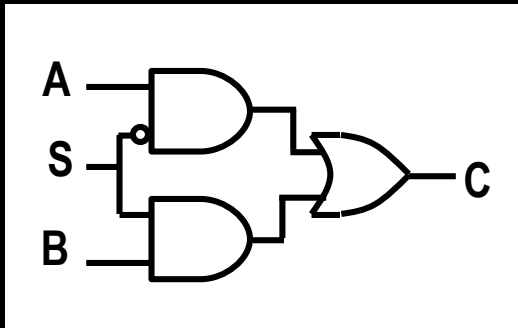


# EECS 370 Discussion

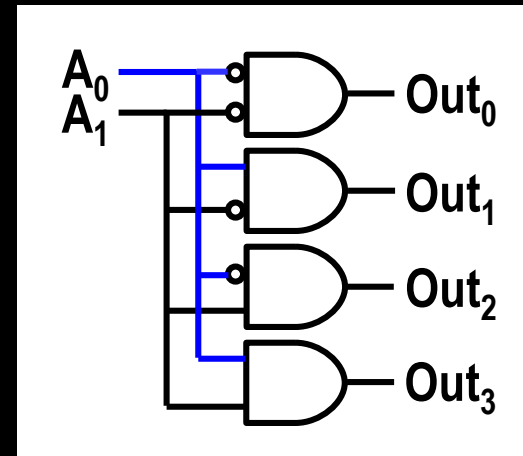
## Combinational Logic

More Complex Circuits:

Mux



Decoder

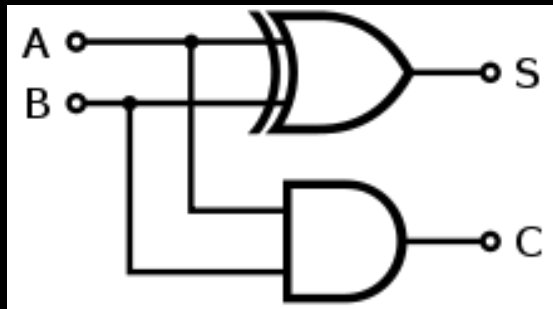


# EECS 370 Discussion

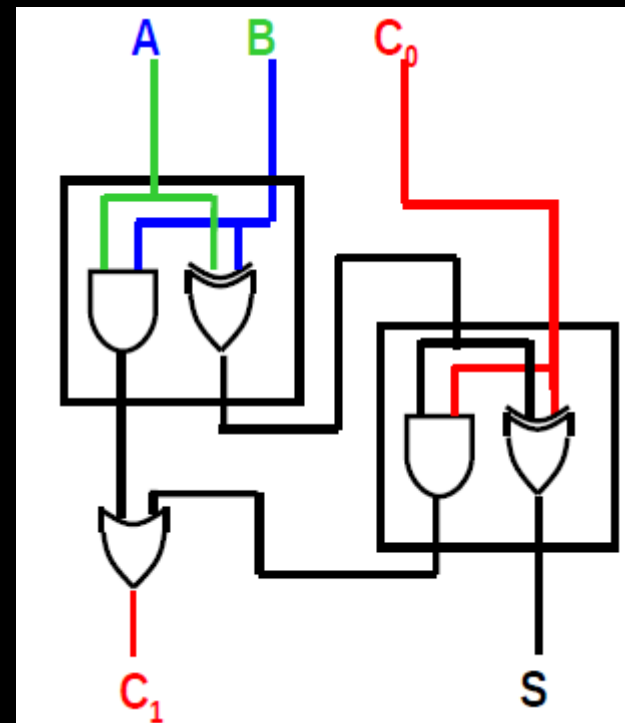
## Combinational Logic

More Complex Circuits:

Half Adder



Full Adder

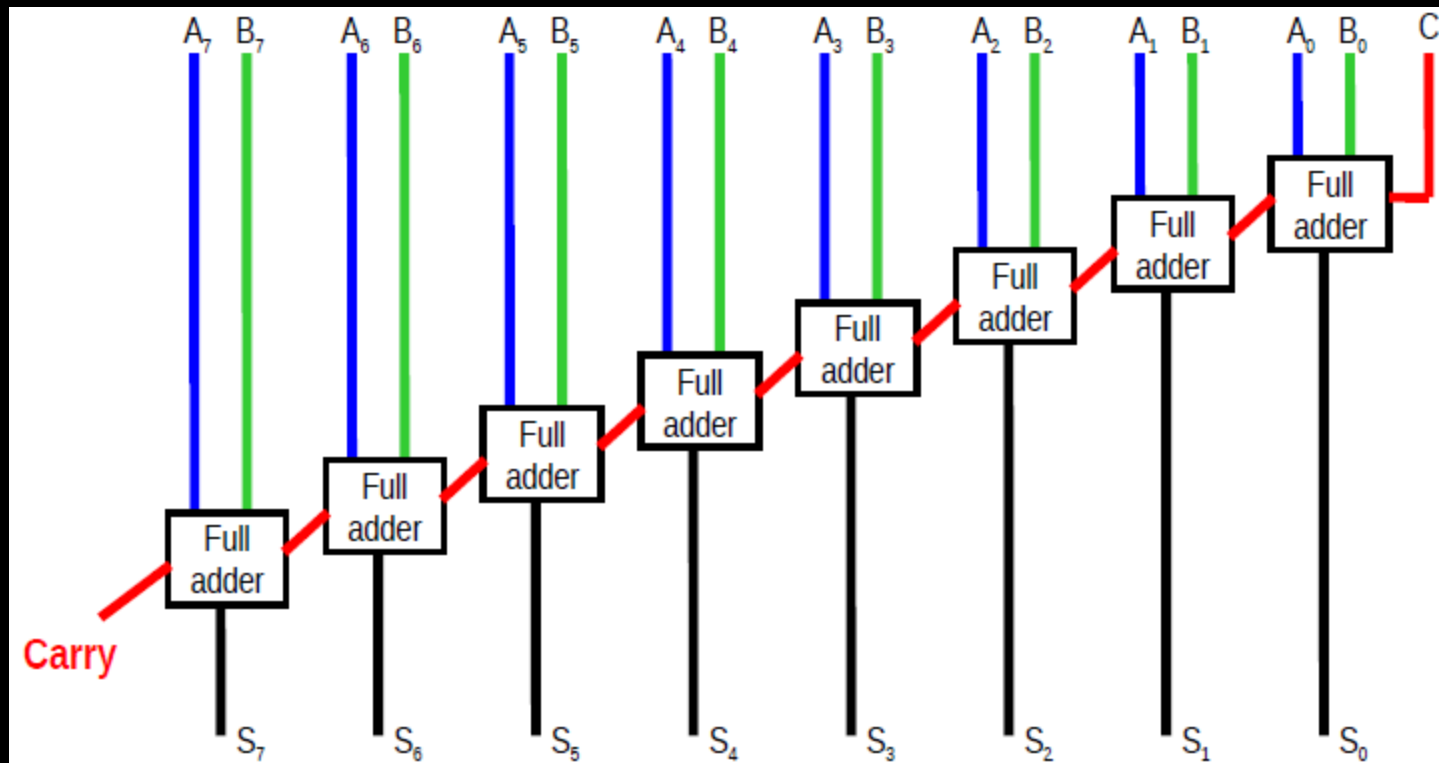


# EECS 370 Discussion

## Combinational Logic

More Complex Circuits:

### Ripple Carry Adder

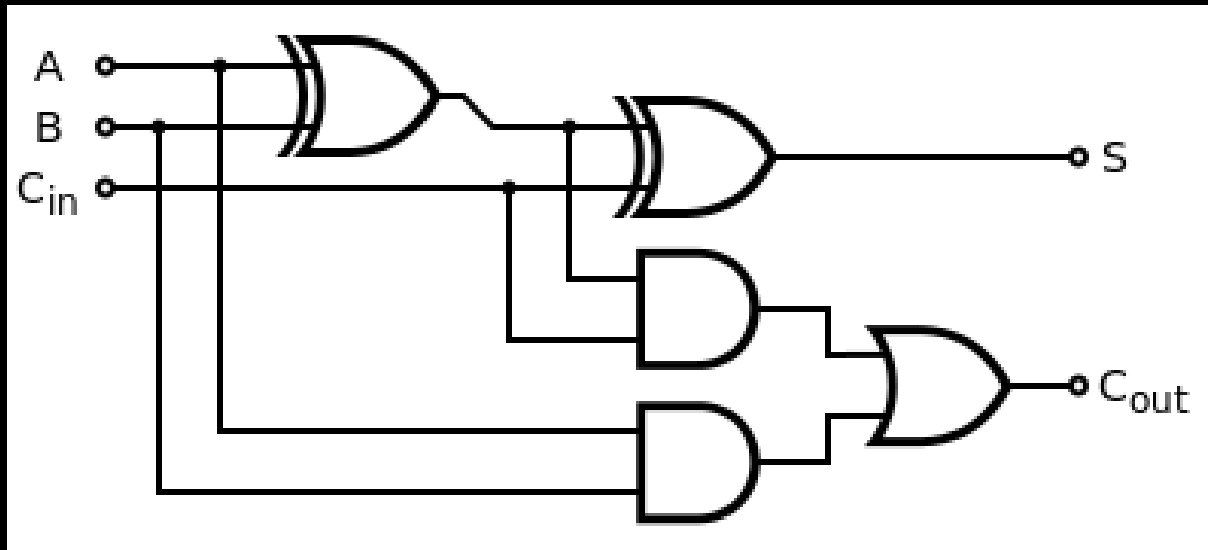




# EECS 370 Discussion

## Combinational Logic

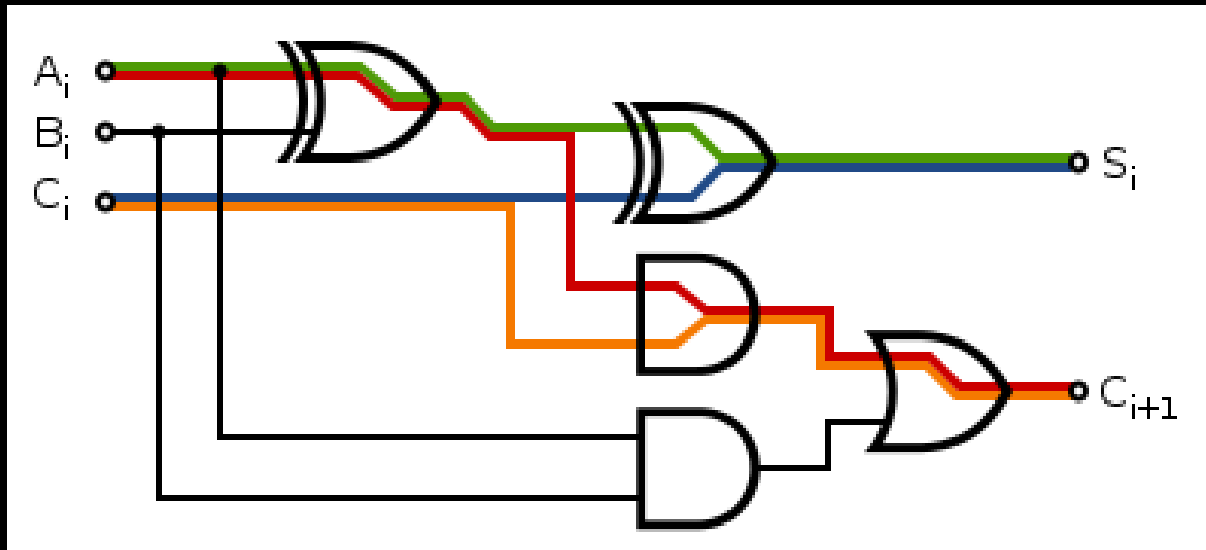
### Propagation Delay



# EECS 370 Discussion

## Combinational Logic

### Propagation Delay



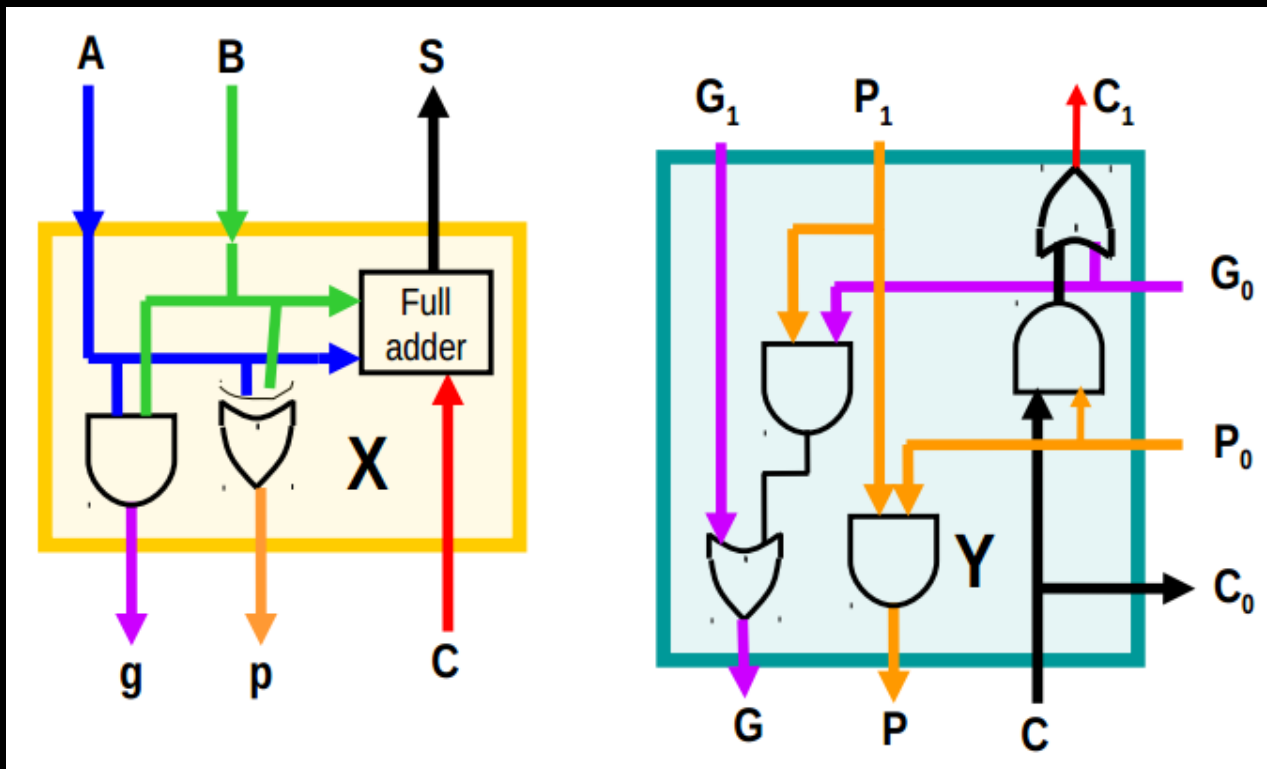
Slows down the speed of your circuit!

# EECS 370 Discussion

## Combinational Logic

Most Complex Circuits:

Carry Look-ahead Adder



# EECS 370 Discussion

## Sequential Logic

### Combinational Logic

Stateless

Output is direct function of current input

### Sequential Logic

Stateful

Output is function of current input and past input

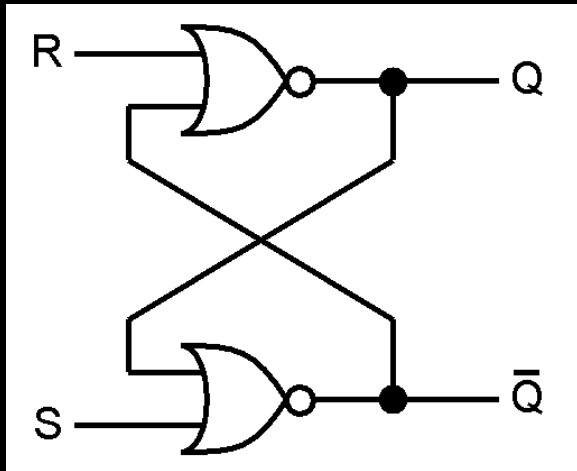
Clocked!

# EECS 370 Discussion

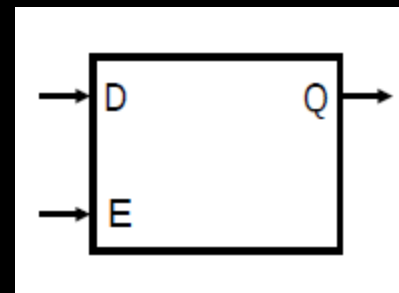
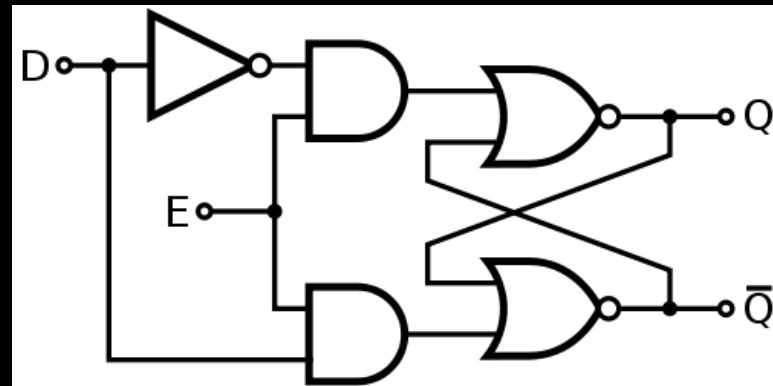
## Sequential Logic

### Latches

SR Latch



D Latch

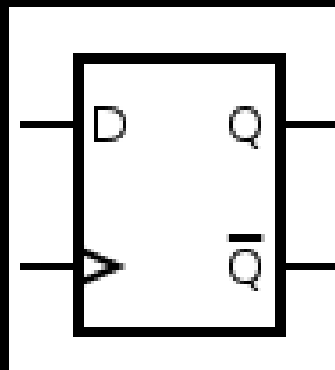
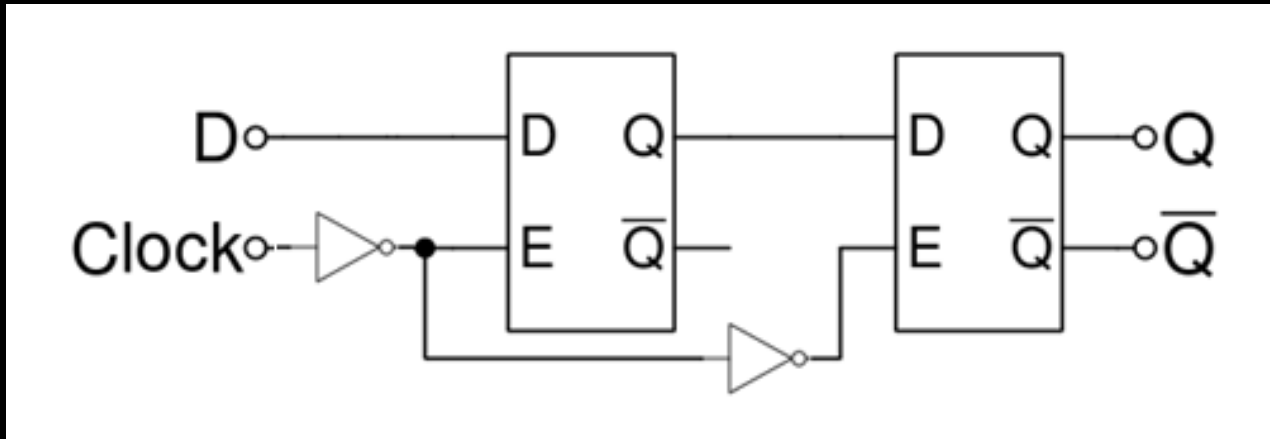


# EECS 370 Discussion

## Sequential Logic

### Flip Flops

#### Positive Edge Triggered



# EECS 370 Discussion

## Sequential Logic

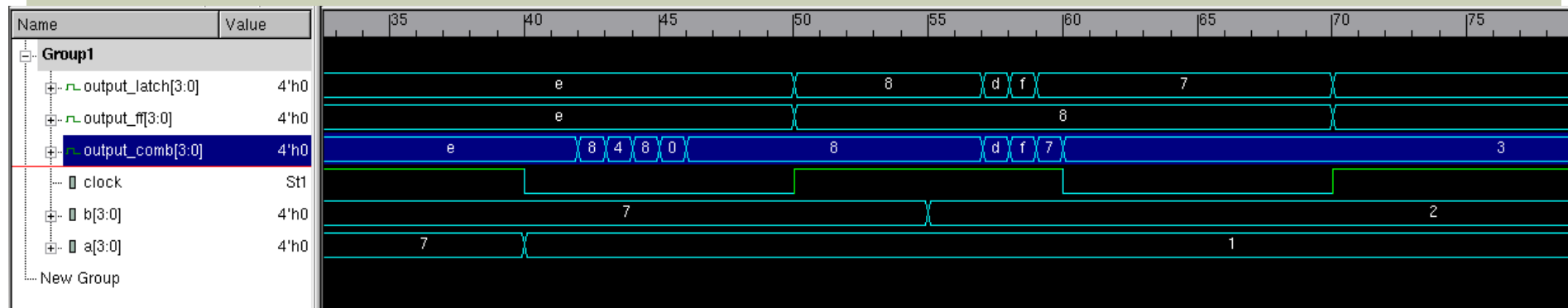
Why do we want clocked logic?

Specifies a time by which all operations are “done”

Results before that time do not matter

# AN EXAMPLE OF WHY THIS MATTERS

- Delays in combinational circuits are very real.

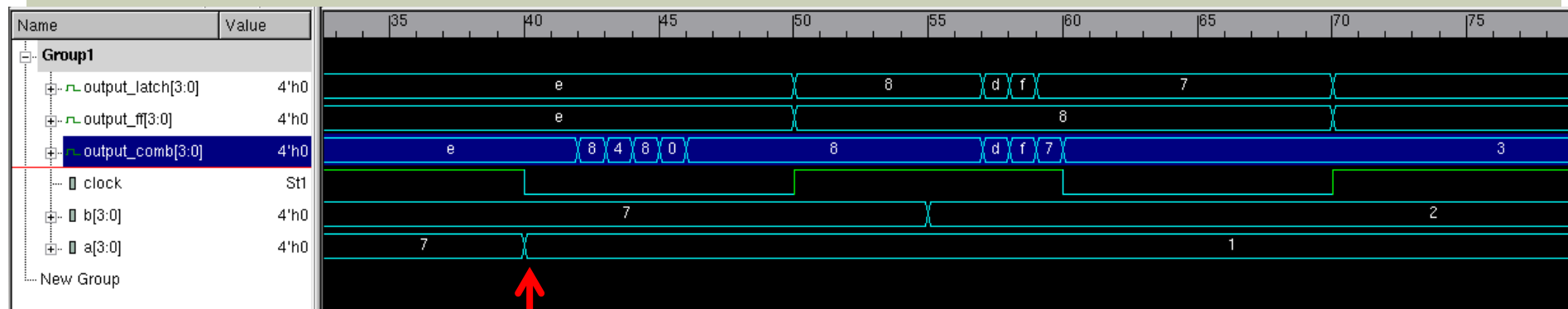


- Here's an example with a ripple carry adder.



# AN EXAMPLE OF WHY THIS MATTERS

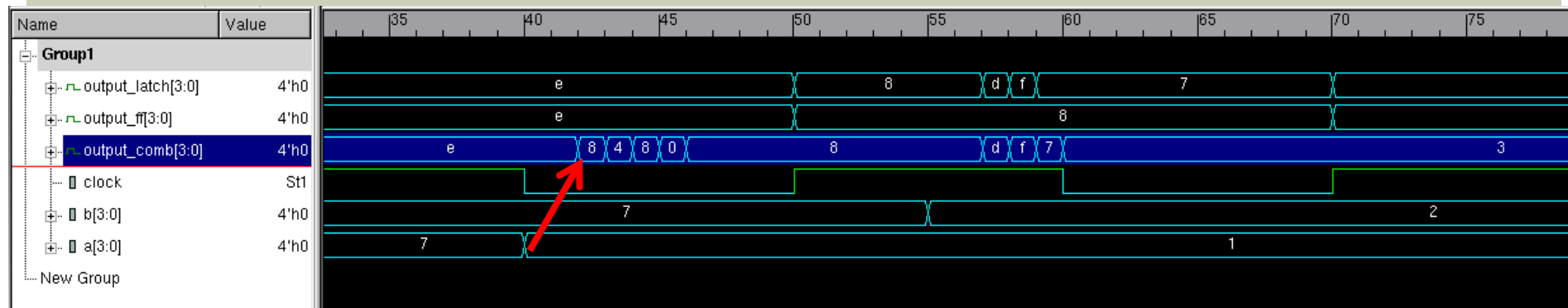
- Let's zoom in on the interesting part.



The value of a goes from 7 to 1 here

# AN EXAMPLE OF WHY THIS MATTERS

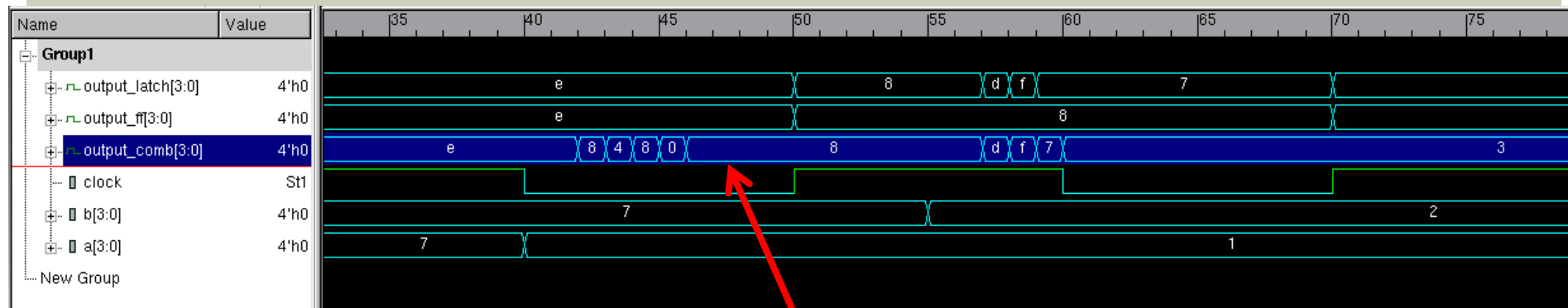
- Let's zoom in on the interesting part.



There's propagation delay before the adder even starts to change values.

# AN EXAMPLE OF WHY THIS MATTERS

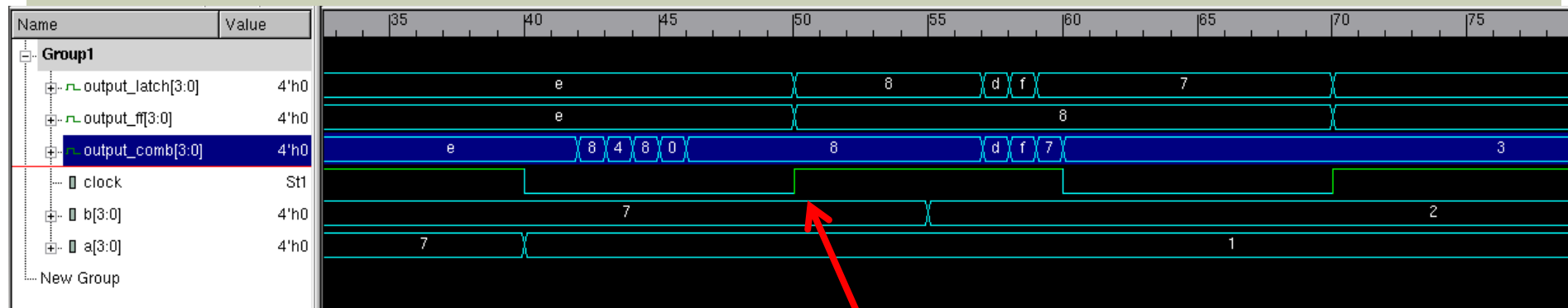
- Let's zoom in on the interesting part.



The value stabilizes

# AN EXAMPLE OF WHY THIS MATTERS

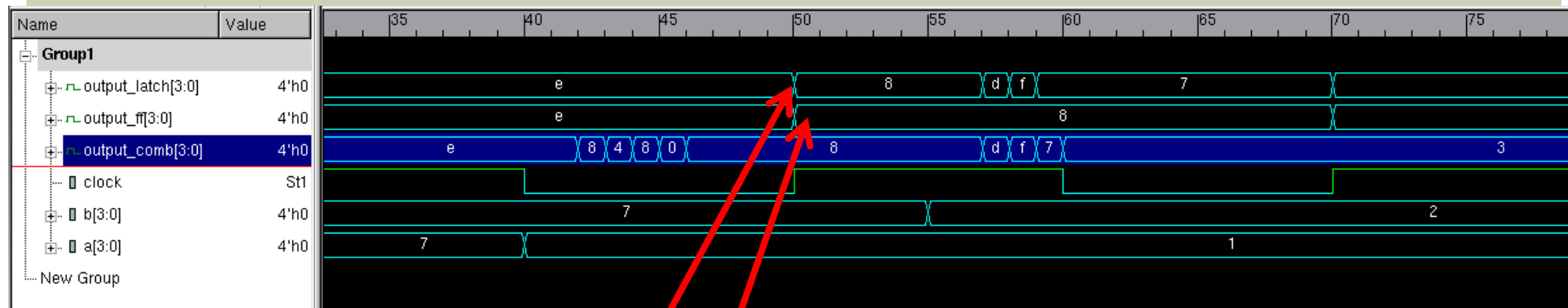
- Let's zoom in on the interesting part.



The next clock edge comes along

# AN EXAMPLE OF WHY THIS MATTERS

- Let's zoom in on the interesting part.

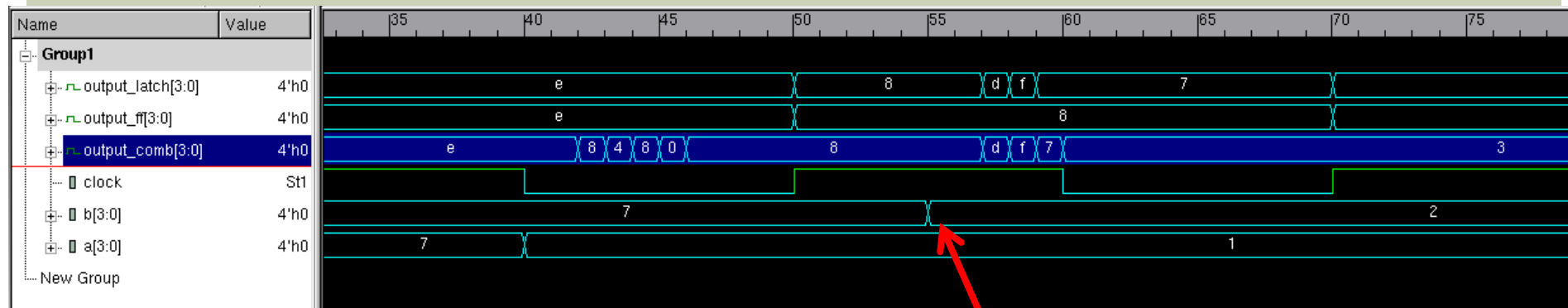


The latch opens up  
(and shows new value)

The flip-flop grabs new value.

# AN EXAMPLE OF WHY THIS MATTERS

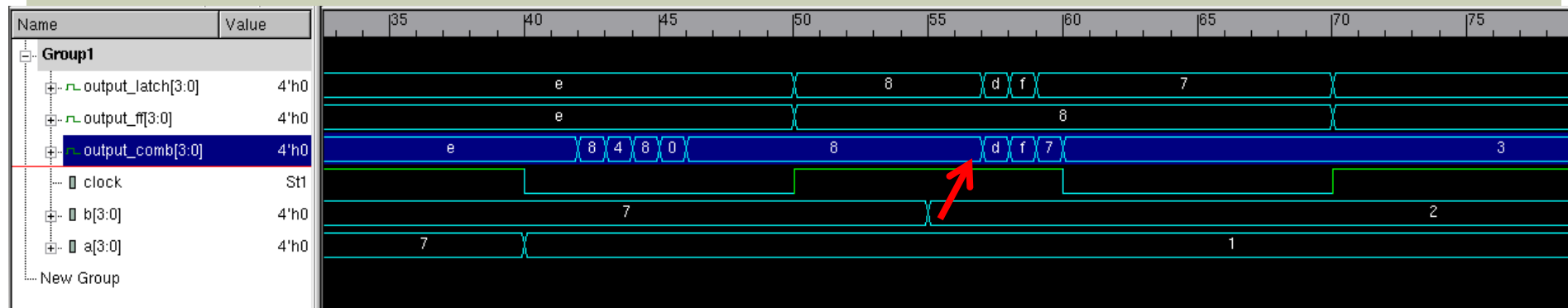
- Let's zoom in on the interesting part.



**B changes now,  
while the clock is still high.**

# AN EXAMPLE OF WHY THIS MATTERS

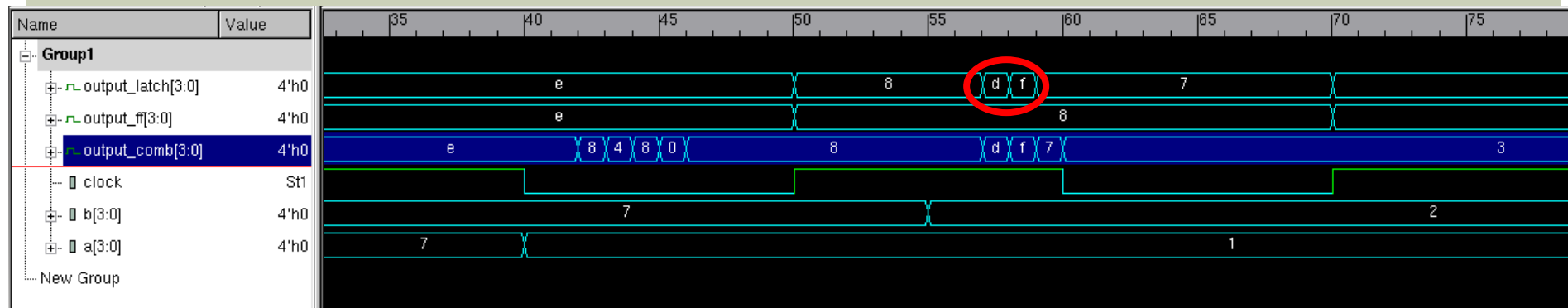
- Let's zoom in on the interesting part.



Again, there's propagation delay before the adder starts to change.

# AN EXAMPLE OF WHY THIS MATTERS

- Let's zoom in on the interesting part.

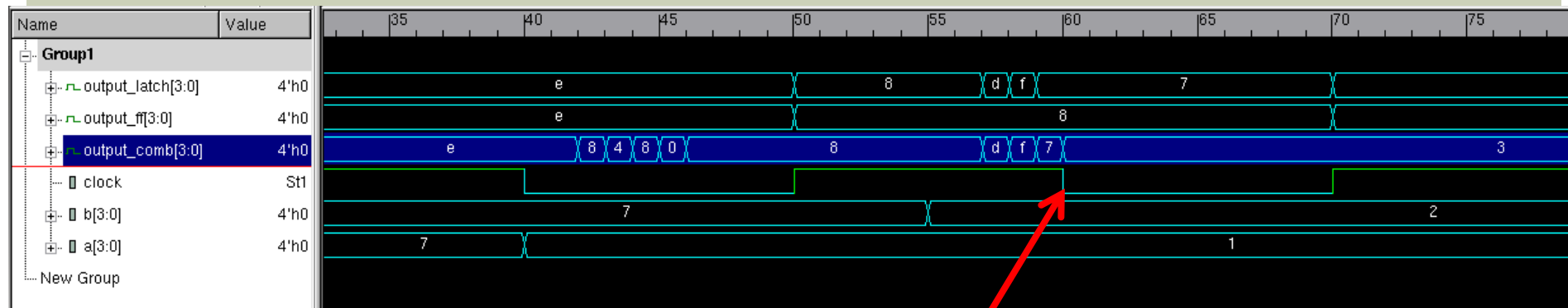


The value in the latch changes too!



# AN EXAMPLE OF WHY THIS MATTERS

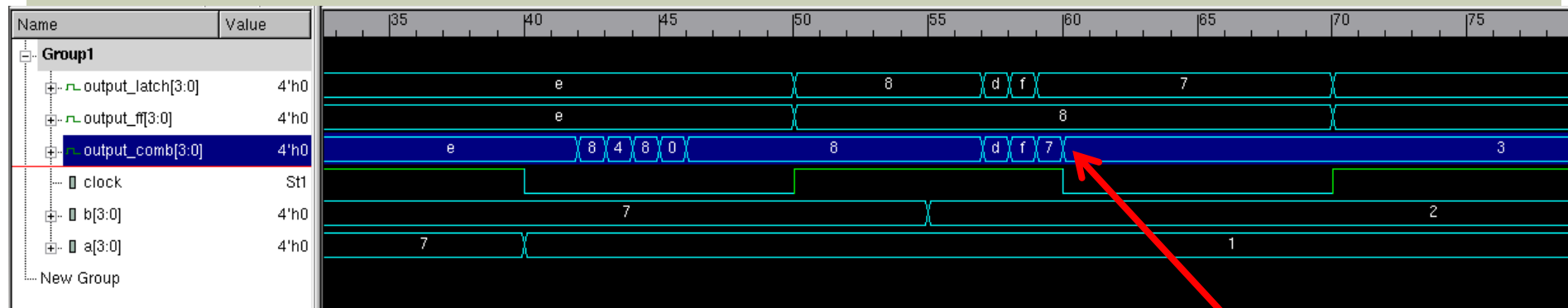
- Let's zoom in on the interesting part.



The next falling edge comes along

# AN EXAMPLE OF WHY THIS MATTERS

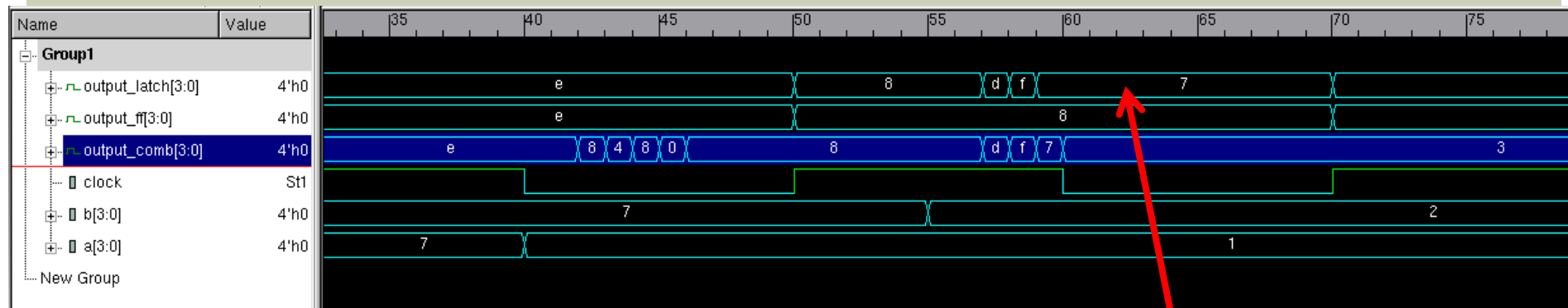
- Let's zoom in on the interesting part.



The adder stabilizes.

# AN EXAMPLE OF WHY THIS MATTERS

- Let's zoom in on the interesting part.



The latch locked with the wrong value!