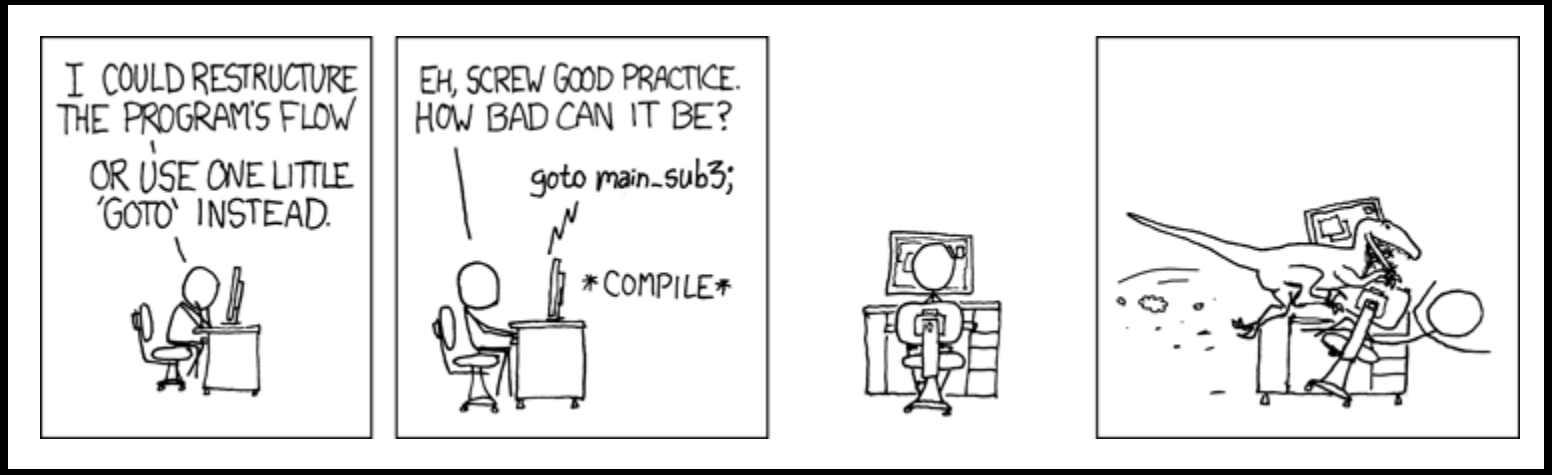
EECS 370 Discussion



xkcd.com

EECS 370 Discussion

Mid-semester Feedback

- Thanks!

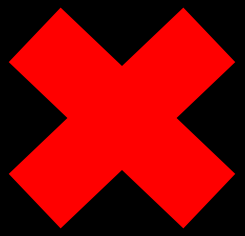
EECS 370 Discussion

Topics Today:

- Multi-cycle Datapath
- Project 2
- Exams

EECS 370 Discussion

Exam Results

- Answer Keys are posted online
- Exams will be returned  next week

EECS 370 Discussion

Multi-Cycle Datapath

Key Concepts

- Is the frequency of the processor Higher or Lower than Single Cycle?

- Will any individual instruction take the same amount of time to complete?

EECS 370 Discussion

Multi-Cycle Datapath

Key Concepts

- Is the frequency of the processor Higher or Lower than Single Cycle?

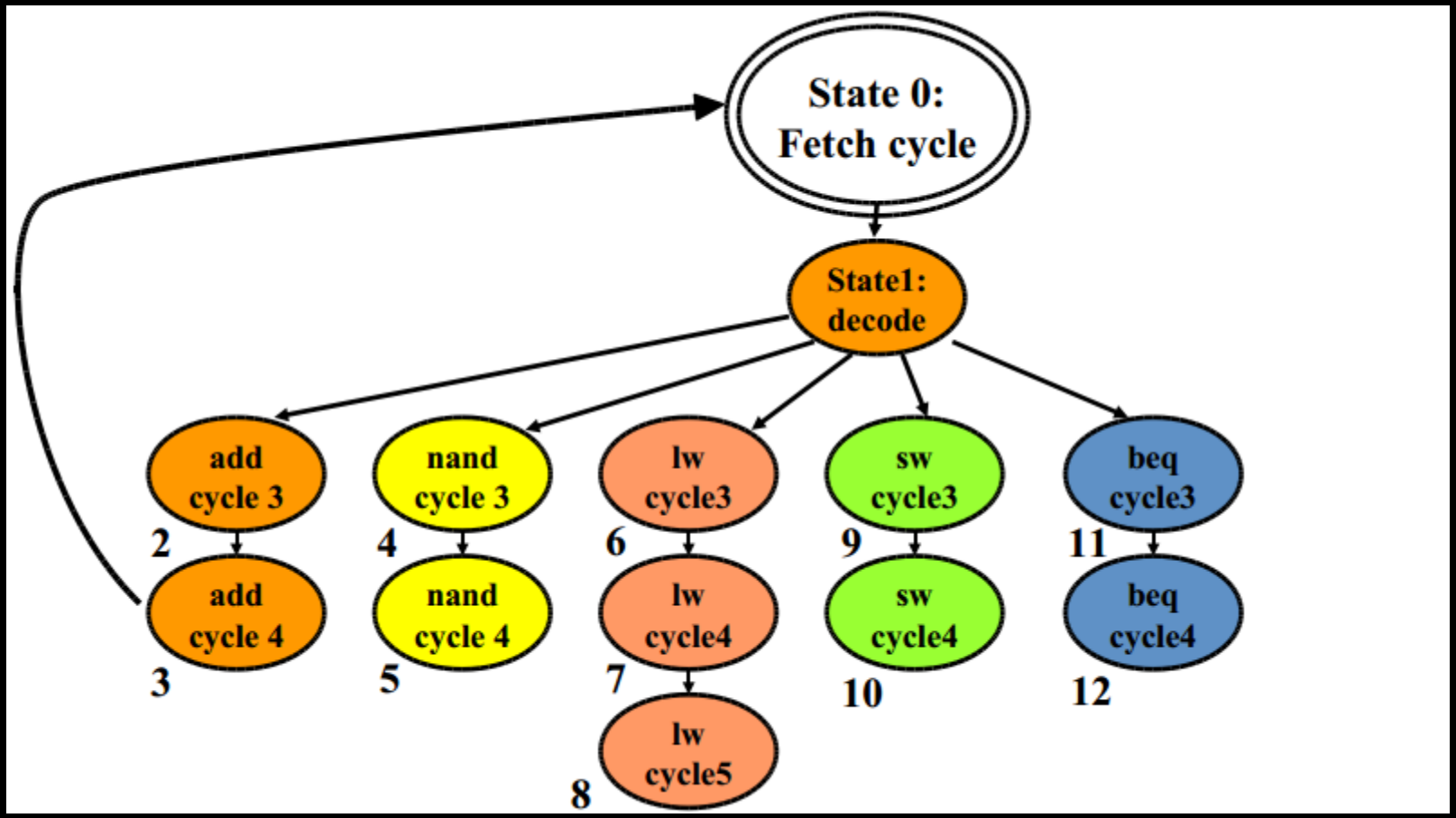
  HIGHER (each stage is simpler)

- Will any individual instruction take the same amount of time to complete?

  NO (some have more states than others)

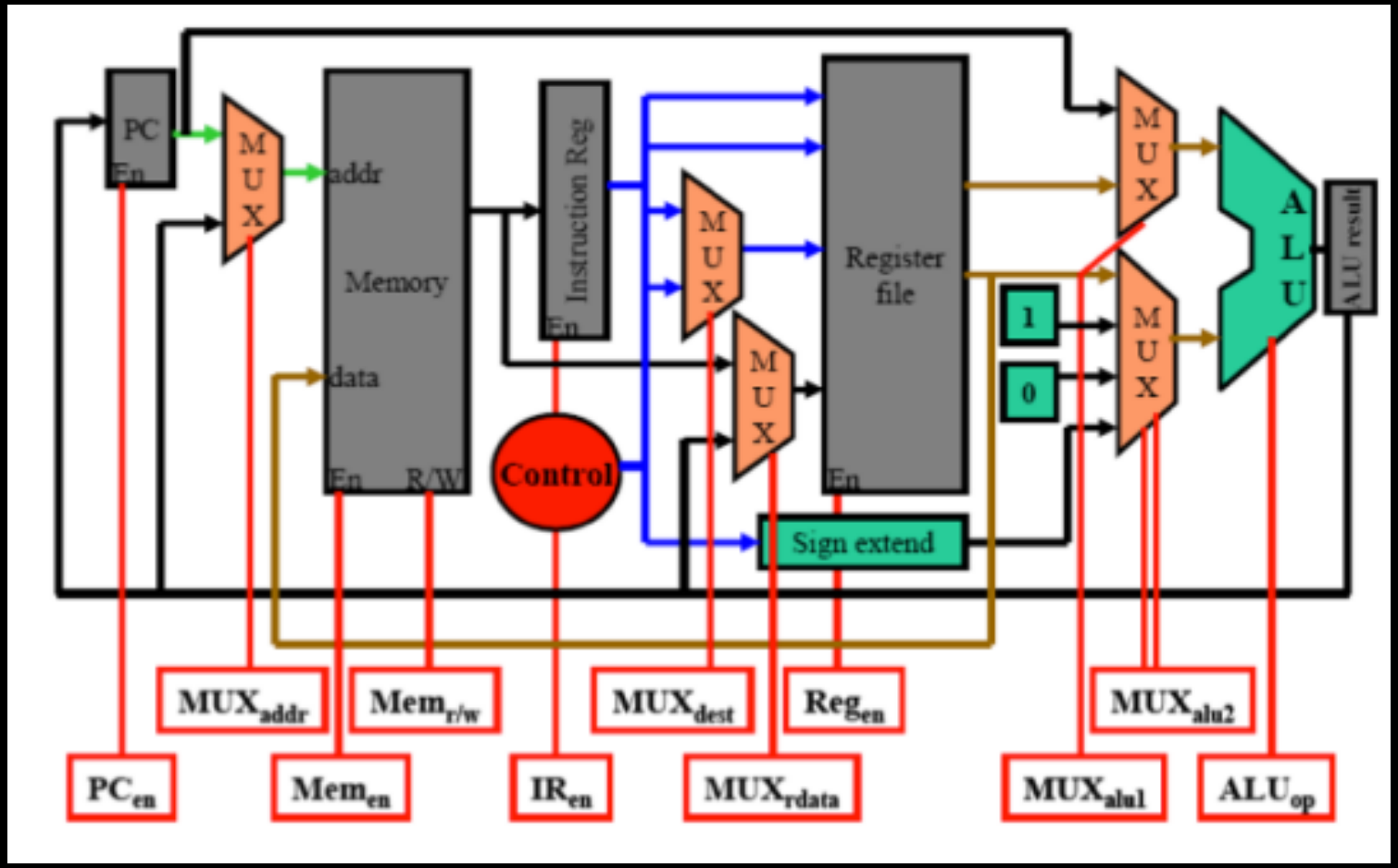
EECS 370 Discussion

Multi-Cycle Datapath



EECS 370 Discussion

Multi-Cycle Datapath



EECS 370 Discussion

Multi-Cycle Datapath

Timing Example

5 ns – Register Read/Write
10 ns – ALU Operations
20 ns – Memory Access

Single Cycle Processor

Inst	I-Mem Access	Read Register	ALU Operation	D-Mem Access	Write Register	Cycle Time
add	✓	✓	✓		✓	
nand	✓	✓	✓		✓	
lw	✓	✓	✓	✓	✓	
sw	✓	✓	✓	✓		
beq	✓	✓	✓			

EECS 370 Discussion

Multi-Cycle Datapath

Timing Example

5 ns – Register Read/Write
10 ns – ALU Operations
20 ns – Memory Access

Single Cycle Processor

Inst	I-Mem Access	Read Register	ALU Operation	D-Mem Access	Write Register	Cycle Time
add	✓	✓	✓		✓	40 ns
nand	✓	✓	✓		✓	40 ns
lw	✓	✓	✓	✓	✓	60 ns
sw	✓	✓	✓	✓		55 ns
beq	✓	✓	✓			35 ns

EECS 370 Discussion

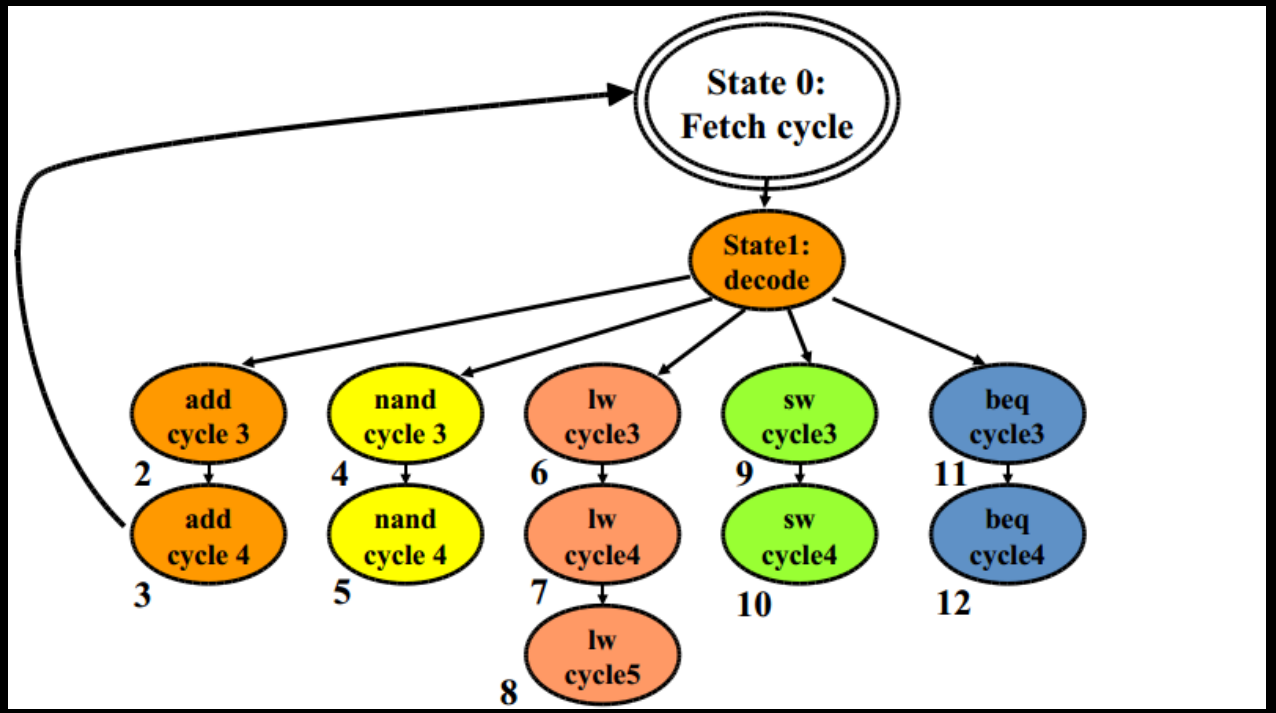
Multi-Cycle Datapath

Timing Example

5 ns – Register Read/Write
10 ns – ALU Operations
20 ns – Memory Access

Multi Cycle Processor

Inst	Number of Cycles
add	
nand	
lw	
sw	
beq	



EECS 370 Discussion

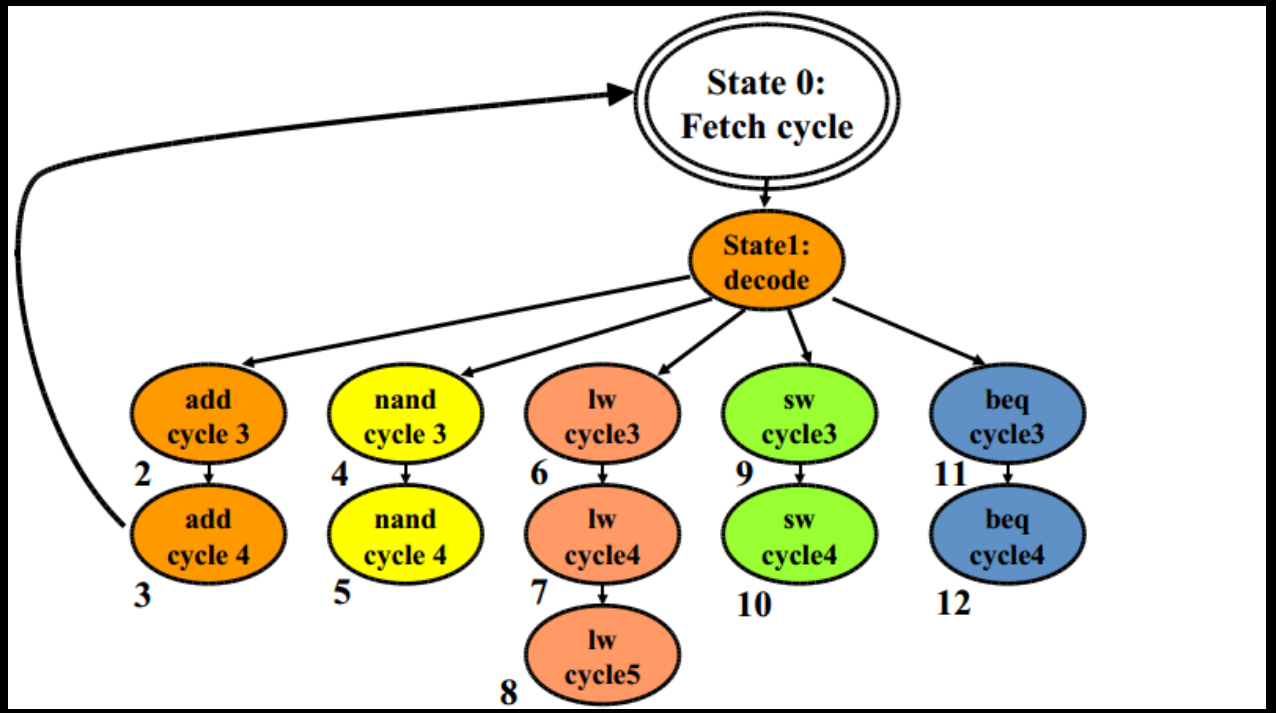
Multi-Cycle Datapath

Timing Example

5 ns – Register Read/Write
10 ns – ALU Operations
20 ns – Memory Access

Multi Cycle Processor

Inst	Number of Cycles
add	4
nand	4
lw	5
sw	4
beq	4



EECS 370 Discussion

Multi-Cycle Datapath

Timing Example

5 ns – Register Read/Write
10 ns – ALU Operations
20 ns – Memory Access

Multi Cycle Processor

Inst	Number of Cycles
add	4
nand	4
lw	5
sw	4
beq	4

What is our cycle time?

EECS 370 Discussion

Multi-Cycle Datapath

Timing Example

5 ns – Register Read/Write
10 ns – ALU Operations
20 ns – Memory Access

Multi Cycle Processor

Inst	Number of Cycles
add	4
nand	4
lw	5
sw	4
beq	4

What is our cycle time?

20 ns

EECS 370 Discussion

Multi-Cycle Datapath

Timing Example

100 Instructions:

35% lw
15% sw
40% add/nand
20% beq

What is the total execution time?

Single Cycle:

Multi-Cycle:

EECS 370 Discussion

Multi-Cycle Datapath

Timing Example

100 Instructions:

35% lw
15% sw
30% add/nand
20% beq

What is the total execution time?

Single Cycle: 100 * 60 = 6000 ns

Multi-Cycle: 20 * (35*5 + 15*4 + 30*4 + 20*4) = 8700 ns

EECS 370 Discussion

Project 2

Key Concepts

- How many of you have read the project specification?

- Is it the same multi-cycle processor from class?

EECS 370 Discussion

Project 2

Key Concepts

- How many of you have read the project specification?

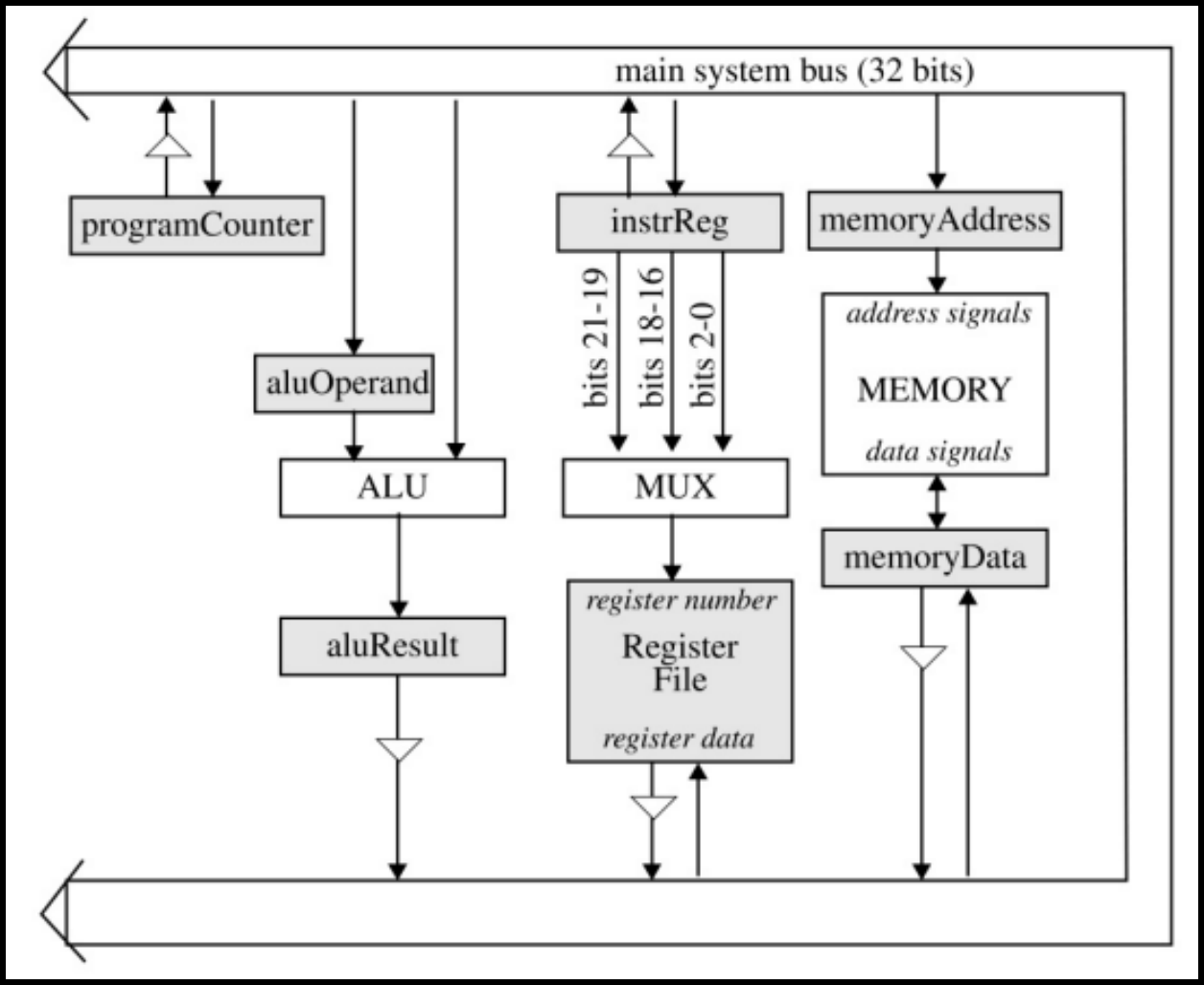
  All of you, cause you're the best students ever!!

- Is it the same multi-cycle processor from class?

  NO

EECS 370 Discussion

Project 2 - Multicycle



EECS 370 Discussion

Project 2 - Multicycle

Illegal State Transitions

- Write to register and read it in same cycle
- Write two different values to bus in same cycle
- Use value on bus from previous cycle
- Use hardware twice in same cycle
  - Memory
  - ALU

EECS 370 Discussion

Project 2 - Multicycle

Commonly Overlooked Optimization

- For PC, don't use the ALU to increment

  state.pc++

EECS 370 Discussion

Project 2 - Combinations

Let's write a function in LC2K assembly

(Caller Saved Registers)

```
int main( ) {
      int a = 2;
      int b = 3;
      int c = func(a, b);
      return c + a;
}
int func(int n, int r) {
      return n+r+1;
}
```

Register	Use
R0	Value 0
R1	Input N
R2	Input R
R3	Return Value
R4	Local Variable
R5	Stack Pointer
R6	Temporary Value
R7	Return Address

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